FIG. 1

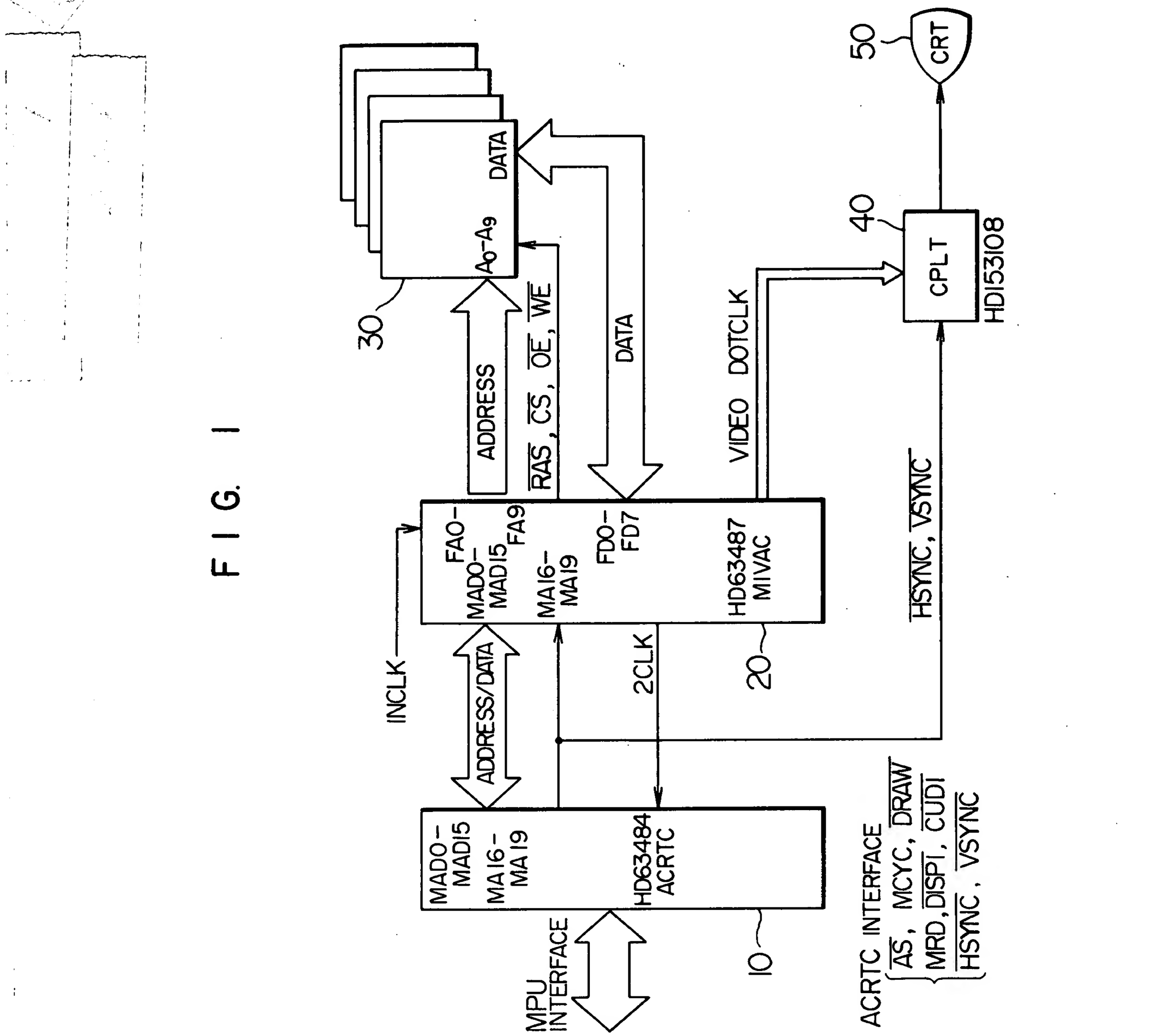

50
CRT
40
CPLT
HD153108
30
DATA
A0-A9
ADDRESS
RAS, CS, OE, WE
DATA
VIDEO DOTCLK
HSYNC, VSYNC
INCLK
FA0-FA9
MA0-MA15
MA16-MA19
FD0-FD7
HD63487 MIVAC
20
2CLK
ADDRESS/DATA
MA0-MA15
MA16-MA19
HD63484 ACRTC
10
MPU INTERFACE
ACRTC INTERFACE
AS, MCYC, DRAW
MRD, DISPI, CUDI
HSYNC, VSYNC

FIG. 2

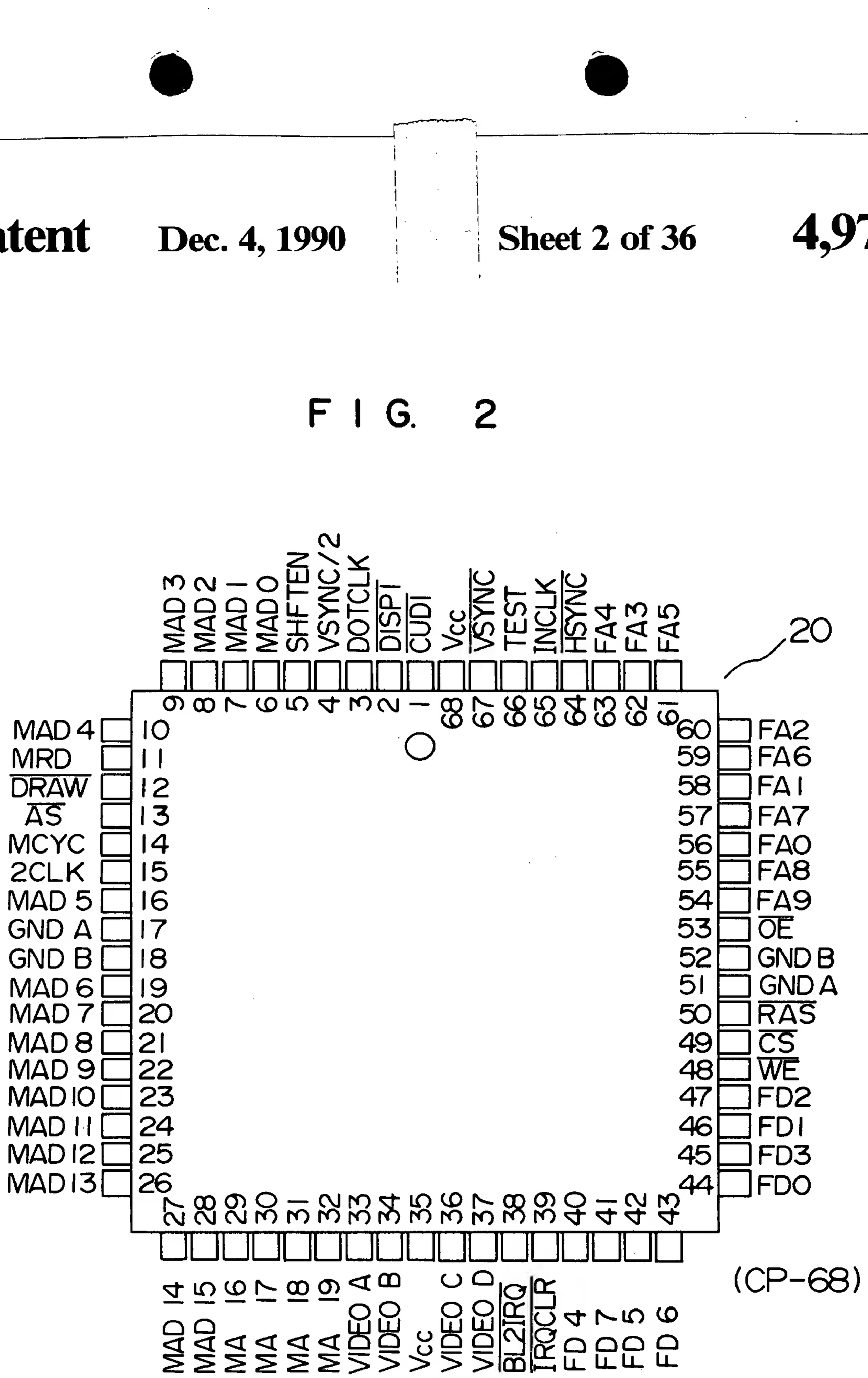

20
MAD 3 9
MAD 2 8
MAD 1 7
MAD 0 6
SHFTEN 5
VSYNC/2 4
DOTCLK 3
DISPI 2
CUDI 1
Vcc 68
VSYNC 67
TEST 66
INCLK 65
HSYNC 64
FA4 63
FA3 62
FA5 61
MAD 4 10
MRD 11
DRAW 12
AS 13
MCYC 14
2CLK 15
MAD 5 16
GND A 17
GND B 18
MAD 6 19
MAD 7 20
MAD 8 21
MAD 9 22
MAD 10 23
MAD 11 24
MAD 12 25
MAD 13 26
60 FA2
59 FA6
58 FA1
57 FA7
56 FA0
55 FA8
54 FA9
53 OE
52 GND B
51 GND A
50 RAS
49 CS
48 WE
47 FD2
46 FD1
45 FD3
44 FD0
27 MAD 14
28 MAD 15
29 MA 16
30 MA 17
31 MA 18
32 MA 19
33 VIDEO A
34 VIDEO B
35 Vcc
36 VIDEO C
37 VIDEO D
38 BL2IRQ
39 IRQCLR
40 FD 4
41 FD 7
42 FD 5
43 FD 6
(CP-68)

FIG. 3a

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC. NAMELY. HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. MCYC INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	$\overline{\text{DRAW}}$	INPUT	$\overline{\text{DRAW}}$ SIGNAL FROM ACRTC IS INPUTTED. $\overline{\text{DRAW}}$ INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. $\overline{\text{DRAW}}$ IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	$\overline{\text{AS}}$	INPUT	$\overline{\text{AS}}$ SIGNAL IS INPUTTED FROM ACRTC $\overline{\text{AS}}$ INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	$\overline{\text{HSYNC}}$	INPUT	$\overline{\text{HSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF $\overline{\text{HSYNC}}$="LOW" AND $\overline{\text{DRAW}}$="HIGH", IF AS PULSE IS RECEIVED, $\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH OPERATION IS CARRIED OUT.
	67	$\overline{\text{VSYNC}}$	INPUT	$\overline{\text{VSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. RECEIVED $\overline{\text{VSYNC}}$ IS DIVIDED BY TWO SO AS TO OUTPUTTED AS VSYNC/2 SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	$\overline{\text{DISP 1}}$	INPUT	$\overline{\text{DISP 1}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{DISP 1}}$ INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	$\overline{\text{CUD1}}$	INPUT	$\overline{\text{CUD 1}}$ SIGNAL IS INPUTTED FROM ACRTIC. $\overline{\text{CUD 1}}$ IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6–10 16 19–28	MAD0 –MAD15	INPUT/OUTPUT	MOD0–MAD15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC="LOW", AS DATA INPUT/OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC="HIGH".
	29-32	MA16–MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16–MA19 IS INPUTTED FROM ACRTC.

FIG. 3b

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	$\overline{RAS}$	OUTPUT	$\overline{RAS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	$\overline{CS}$	OUTPUT	$\overline{CS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	$\overline{WE}$	OUTPUT	$\overline{WE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	$\overline{OE}$	OUTPUT	$\overline{OE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0-FA9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF0-VCF3 AND VMD0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FD0-FD7	INPUT/OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD0-FD3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD0-FD7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 OR 4. DIVISION RATIO IS SET DEPENDING ON VCF0-VCF3 OF ATTRIBUTE CODE.
	33,34 36,37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-DSIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHFTEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF0-VCF3.
	5	SHFTEN	OUTPUT	SHFTEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, $\overline{DISP1}$ FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, $\overline{DISP1}$ IS ELONGATED BACKWARD BY TWO CYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC/2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. $\overline{VSYNC}$ IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	$\overline{BL2IRQ}$	OUTPUT	$\overline{BL2IRQ}$ IS SET BY BLINK2(MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK2 IS AT "HIGH" LEVEL, $\overline{BL2IRQ}$ IS SET TO "LOW" LEVEL.
	39	$\overline{IRQCLR}$	INPUT	$\overline{IRQCLR}$ SIGNAL IS USED TO CLEAR $\overline{BL2IRQ}$ SIGNAL. WHEN "LOW" IS INPUTTED TO $\overline{IRQCLR}$, $\overline{BL2IRQ}$ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

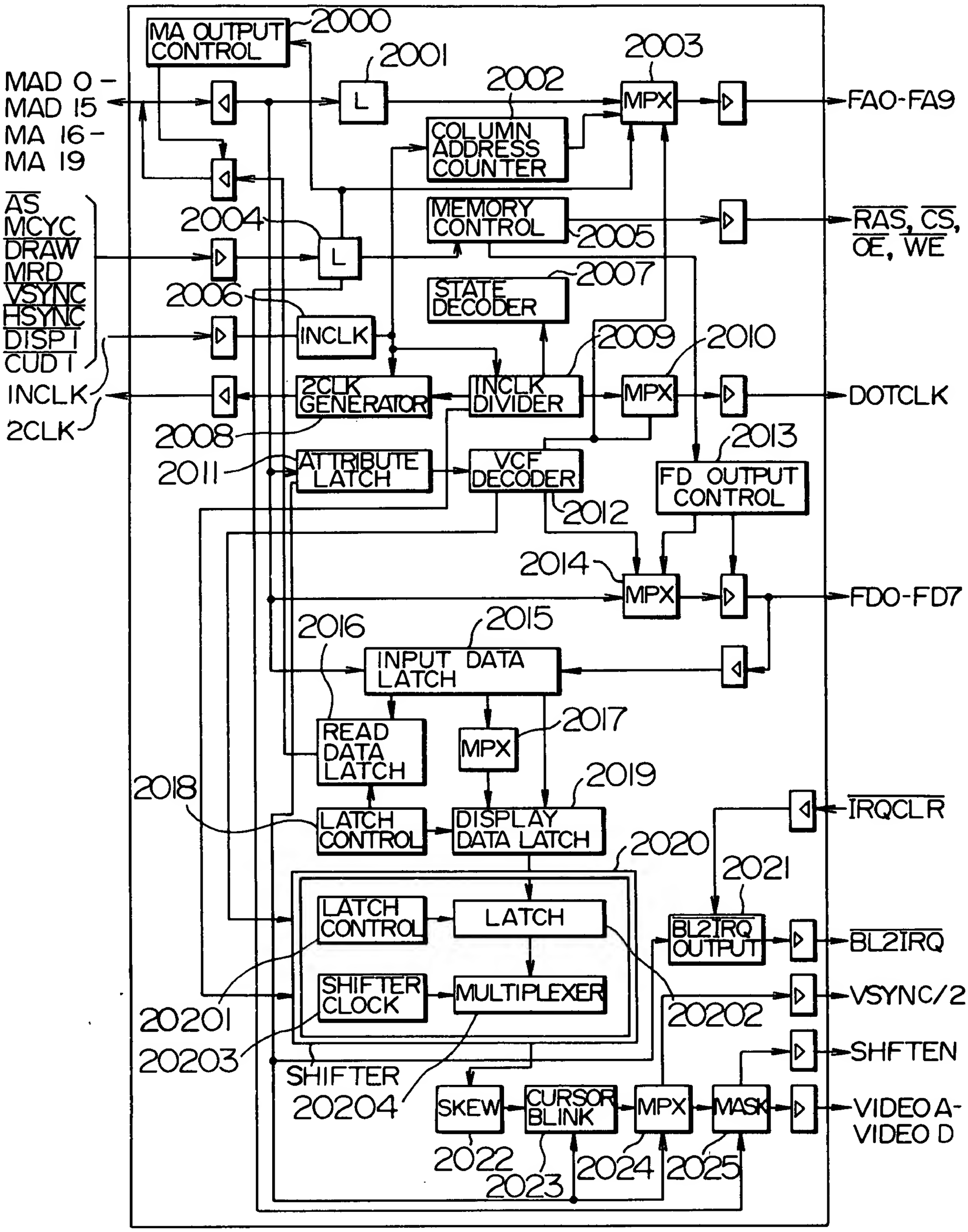

MA OUTPUT CONTROL
2000
2001
2002
2003
MAD 0 - MAD 15
MA 16 - MA 19
L
MPX
FA0-FA9
COLUMN ADDRESS COUNTER
MEMORY CONTROL
2005
RAS, CS, OE, WE
AS
MCYC
DRAW
MRD
VSYNC
HSYNC
DISP1
CUD1
2004
L
2006
STATE DECODER
2007
INCLK
2CLK GENERATOR
INCLK DIVIDER
2009
2010
MPX
DOTCLK
INCLK
2CLK
2008
2011
ATTRIBUTE LATCH
VCF DECODER
2012
2013
FD OUTPUT CONTROL
2014
MPX
FD0-FD7
2016
2015
INPUT DATA LATCH
READ DATA LATCH
MPX
2017
2018
2019
LATCH CONTROL
DISPLAY DATA LATCH
IRQCLR
2020
2021
LATCH CONTROL
LATCH
BL2IRQ OUTPUT
BL2IRQ
SHIFTER CLOCK
MULTIPLEXER
VSYNC/2
20201
20202
20203
SHIFTER
SHFTEN
20204
SKEW
CURSOR BLINK
MPX
MASK
VIDEO A-VIDEO D
2022
2023
2024
2025

FIG. 5a

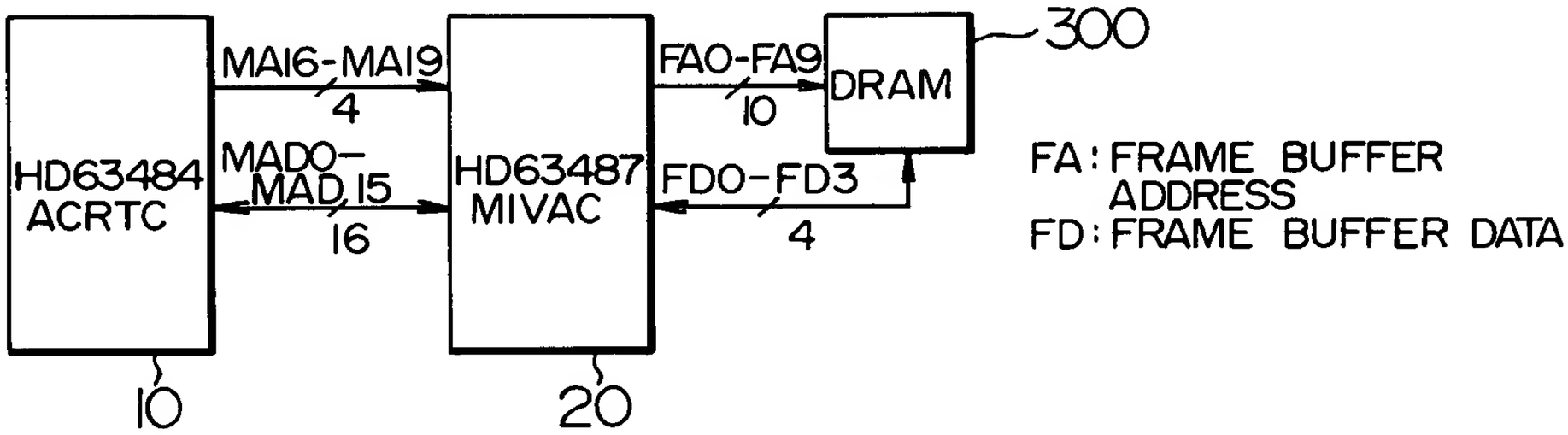


FIG. 5b

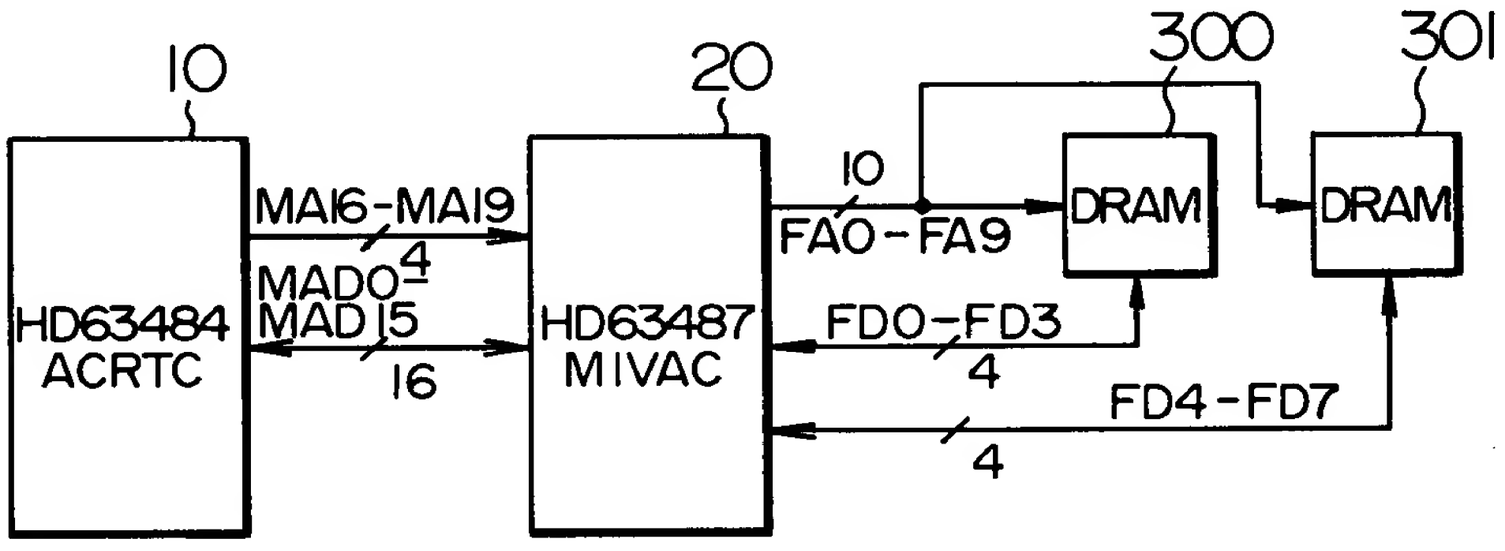


FIG. 5c

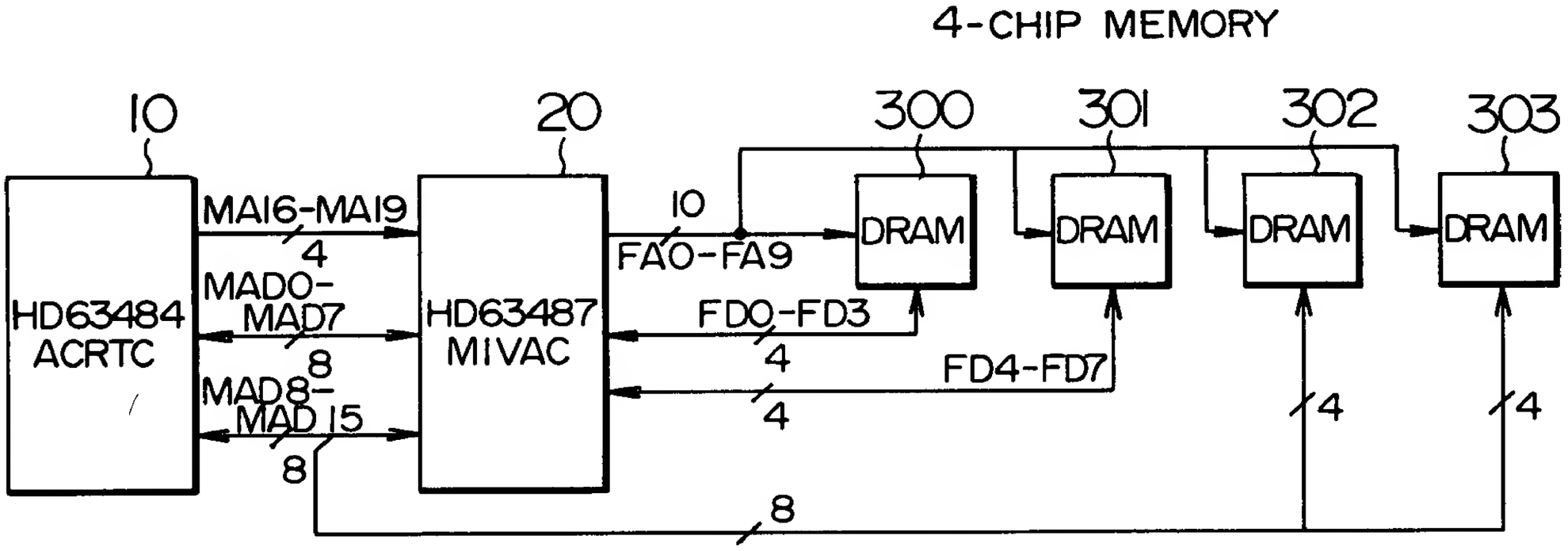


FIG. 6

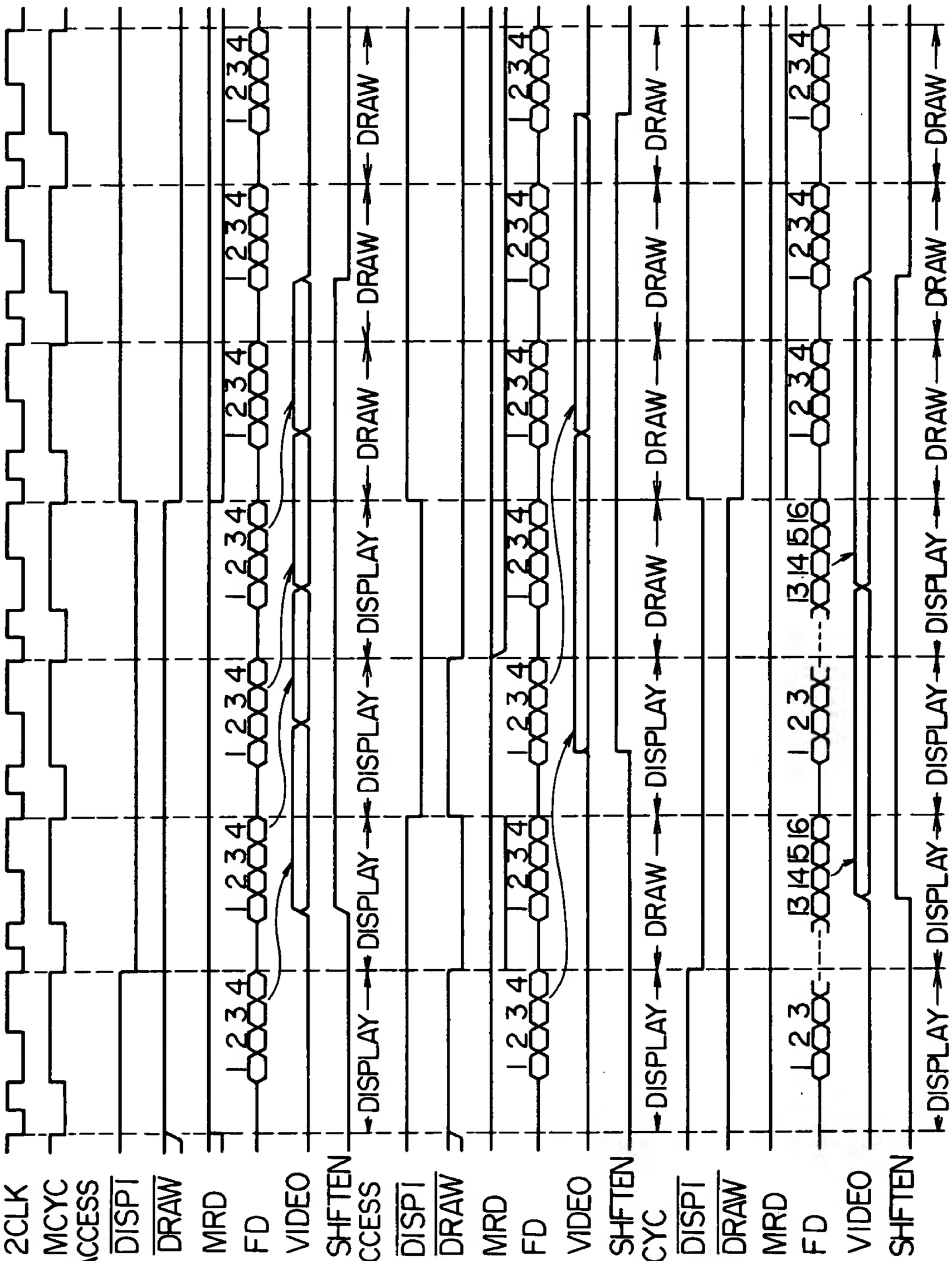

2CLK
MCYC
SINGLE ACCESS
DISPI
DRAW
MRD
FD
VIDEO
SHFTEN
DUAL ACCESS
2MCYC
DISPLAY
DRAW

FIG. 7

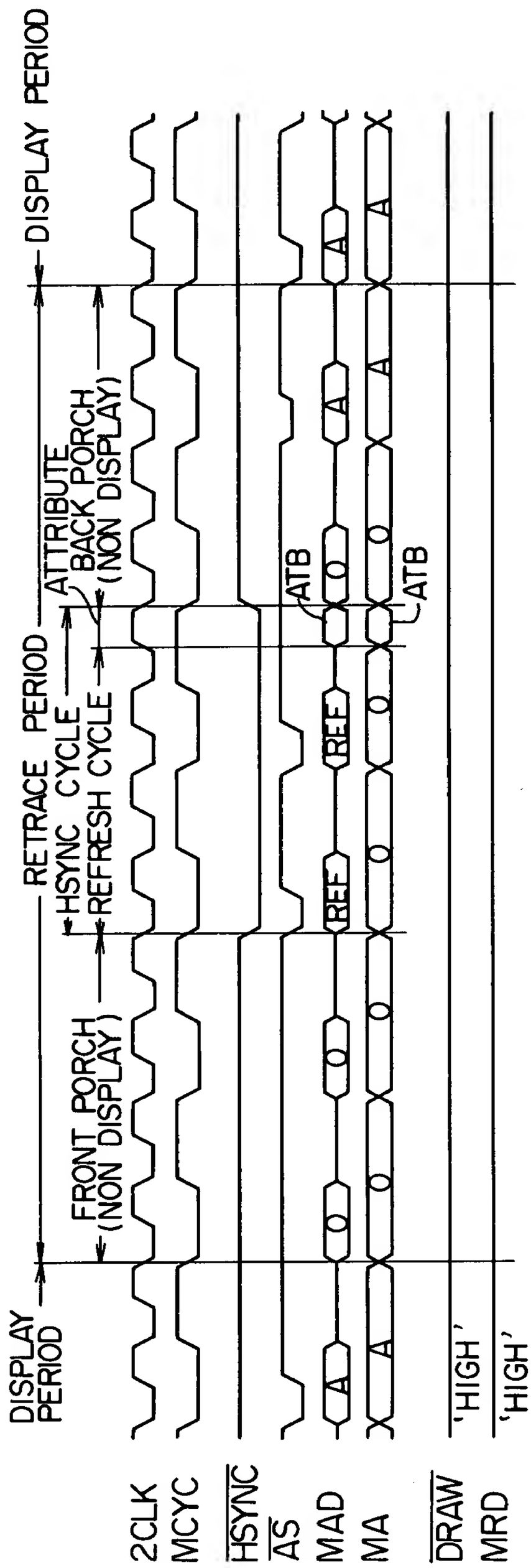


FIG. 11

CUR 1	CUR 0	CURSOR DISPLAY COLOR
0	0	BLACK (VIDEO A – VIDEO D = 0)
0	1	WHITE (VIDEO A – VIDEO D = 1)
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A – VIDEO D
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A–VIDEO C (VIDEO D IS KEPT UNCHANGED)

FIG. 8

MA19	MA18	MA17	MA16	MAD15	~	MAD12	MAD11	~	MAD8	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
BLINK2	BLINK1	SPL2	SPL1	HZ3	~	HZ0	HSD3	~	HSD0	MUXEN	VMD	CUR1	CUR0	VCF3	VCF2	VCF1	VCF0

- BLINK2: $\overline{BL2IRQ}$ OUTPUT IS SET
- BLINK1: BLINKING OF GRAPHIC CURSOR IS SET
- SPL2, SPL1: NOT USED IN MIVAC
- HZ3 ~ HZ0: MULTIPLEXING OF VIDEO OUTPUT IS SET
- HSD3 ~ HSD0: DEPTH OF FRAME BUFFER MEMORY IS SET
- MUXEN: DISPLAY COLOR OF GRAPHIC CURSOR IS SET
- VMD: OPERATION MODE (DISPLAY COLOR, SHIFT AMOUNT OF SHIFT REGISTER, ACCESS MODE, ETC.) OF MIVAC IS SET
- CUR1, CUR0: GRAPHIC CURSOR PATTERN
- VCF3 ~ VCF0: VIDEO CONTROL FLAG

FIG. 9

MODE	CRT SCREEN LAYOUT EXAMPLE (DOTS X RASTER)	MAXIMUM FRAME BUFFER CAPACITY (BYTES)	ACRTC OPERATION FREQUENCY (MHz)	MEMORY ACCESS SPEED	HIGH-SPEED DRAWING	NUMBER OF MEMORIES	COLOR/GRADATION	SHIFT AMOUNT (BITS)	MAXIMUM DOT CLOCK FREQ. (MHz)
0	640x200, 350, 400, 480	512K/128K	4.13	480 ns/4ACCESSES	—	1		16	33
1	640x200, 480x240, 320x200, 240						4	8	16.5
2	320x200, 240 266x192						16	4	8.25
3	640x200, 350, 400, 480	1M/256K				2	4	16	33
4	640x200, 480x240, 320x200, 240						16	8	16.5
5	640x200, 350, 400, 480	2M/512K				4		16	33
6	640x200, 480x240, 320x200, 240	512K/128K			O	1			16.5
7	320x200, 240 256x192,						4	8	8.25
8	640x200, 350, 400, 480	1M/256K				2		32	33
9	640x200, 480x240, 320x200, 240						4	16	16.5
A	320x200, 240 256x192						16	8	8.25
B	640x200, 350, 400, 480	2M/512K				4	4	32	33
C	640x200, 480x240, 320x200, 240						16	16	16.5
D	640x200, 350, 400, 480	512K/128K		960 ns/16ACCESSES	—	1	4	32	33
E	640x200, 480x240, 320x200, 240						16	16	16.5
F	640x200, 350, 400, 480	1M/256K				2		32	33

FIG. 10

MODE	DOT CLOCK FREQUENCY
0, 3, 5, 8 B, D, F	33MHz ~ 11MHz
1, 4, 6, 9 C, E	16.5MHz ~ 5.5MHz
2, 7, A	8.25MHz ~ 2.75MHz

FIG. 12

VMD	MEMORY CHIP EMPLOYED
0	256K × 4BIT DRAM
1	1M × 4BIT DRAM

FIG. 13

MUXEN	VSYNC/2	VIDEO A	VIDEO B
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

FIG. 14

BLINK 1	GRAPHIC CURSOR DISPLAY
0	NOT DISPLAYED
1	DISPLAYED

FIG. 15a

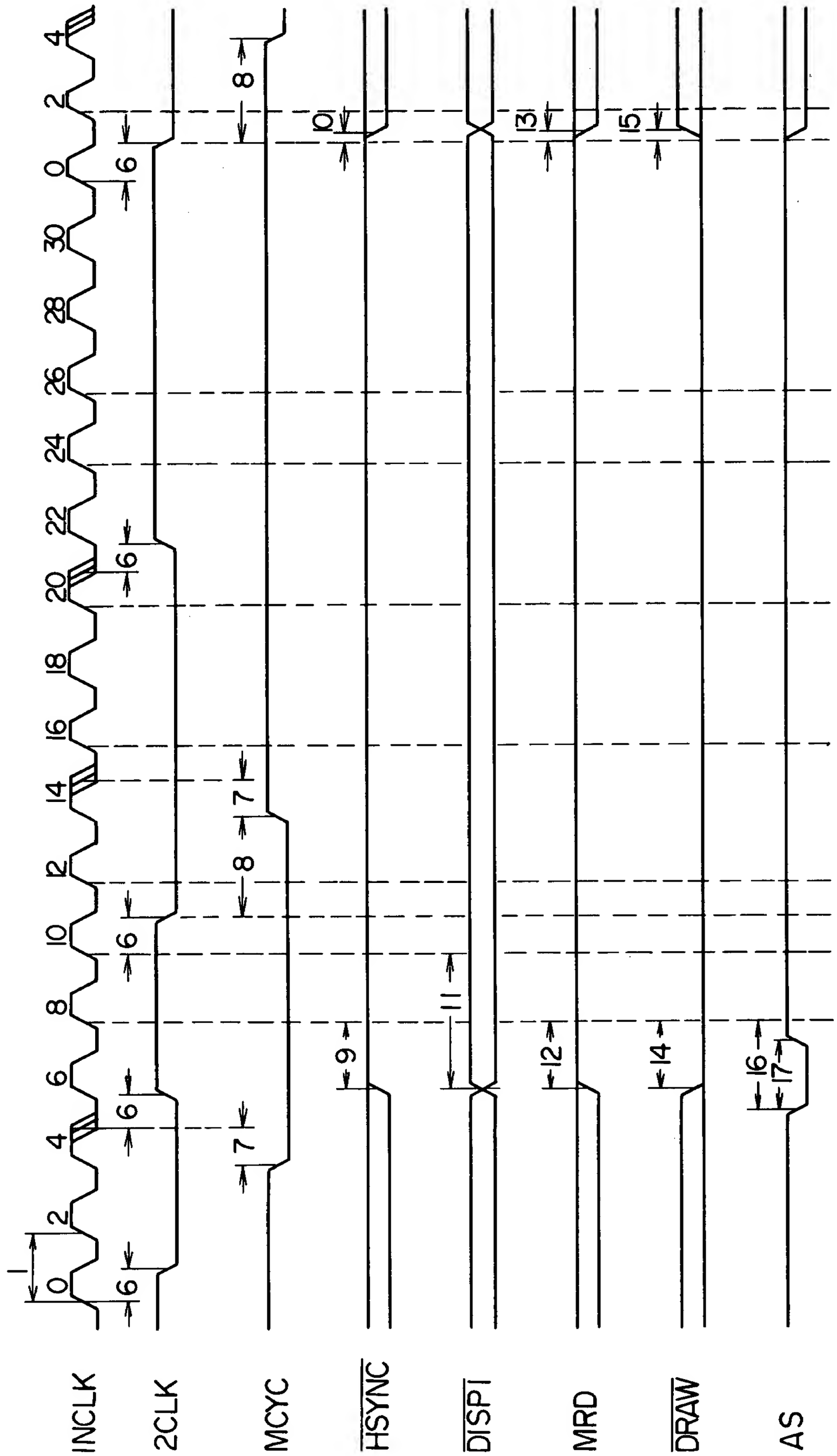
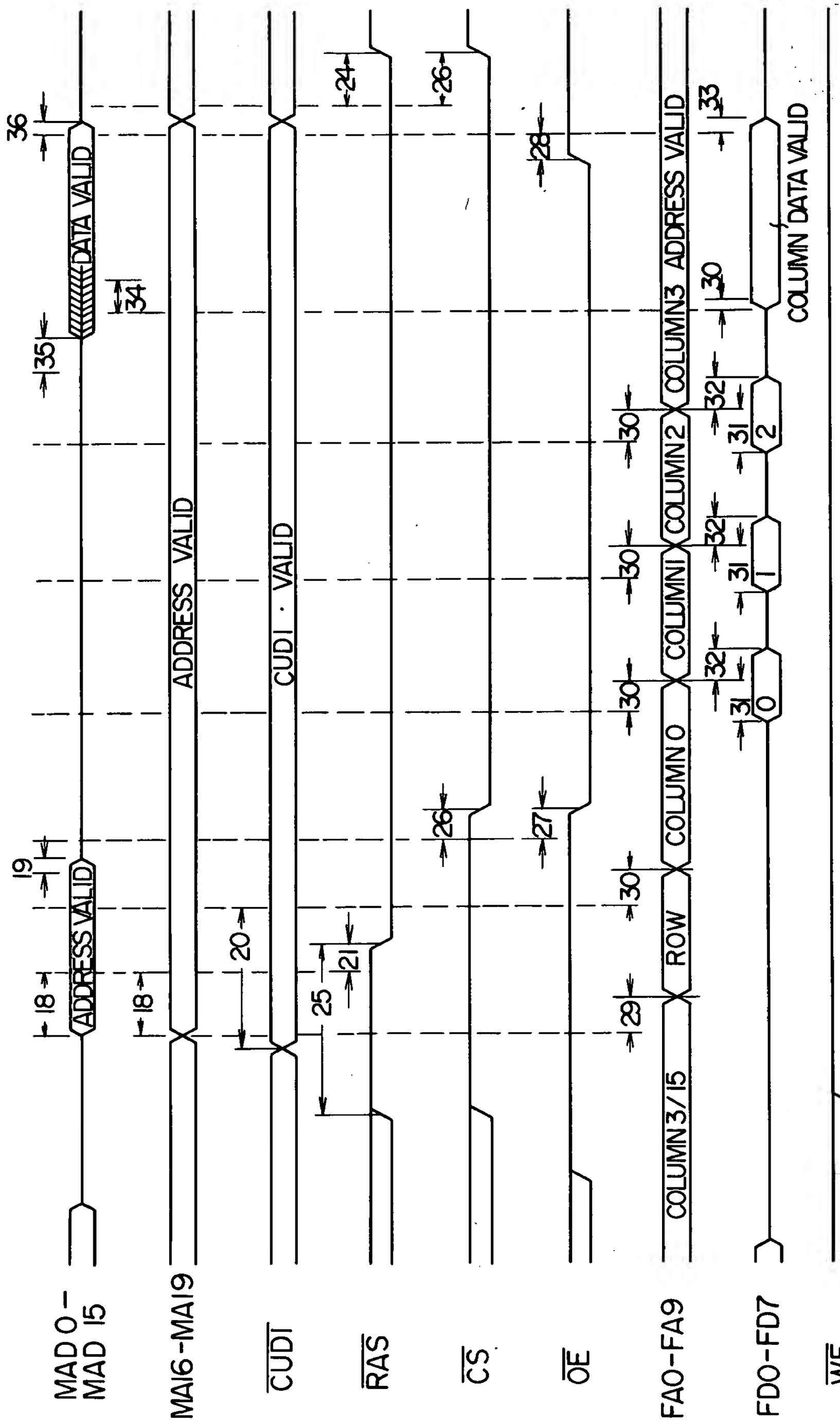


FIG. 15b


MAD 0 – MAD 15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
DATA VALID
CUDI · VALID
COLUMN3 ADDRESS VALID
COLUMN 3/15
ROW
COLUMN 0
COLUMN1
COLUMN2
COLUMN3
0
1
2
18
19
20
21
24
25
26
27
28
29
30
31
32
33
34
35
36

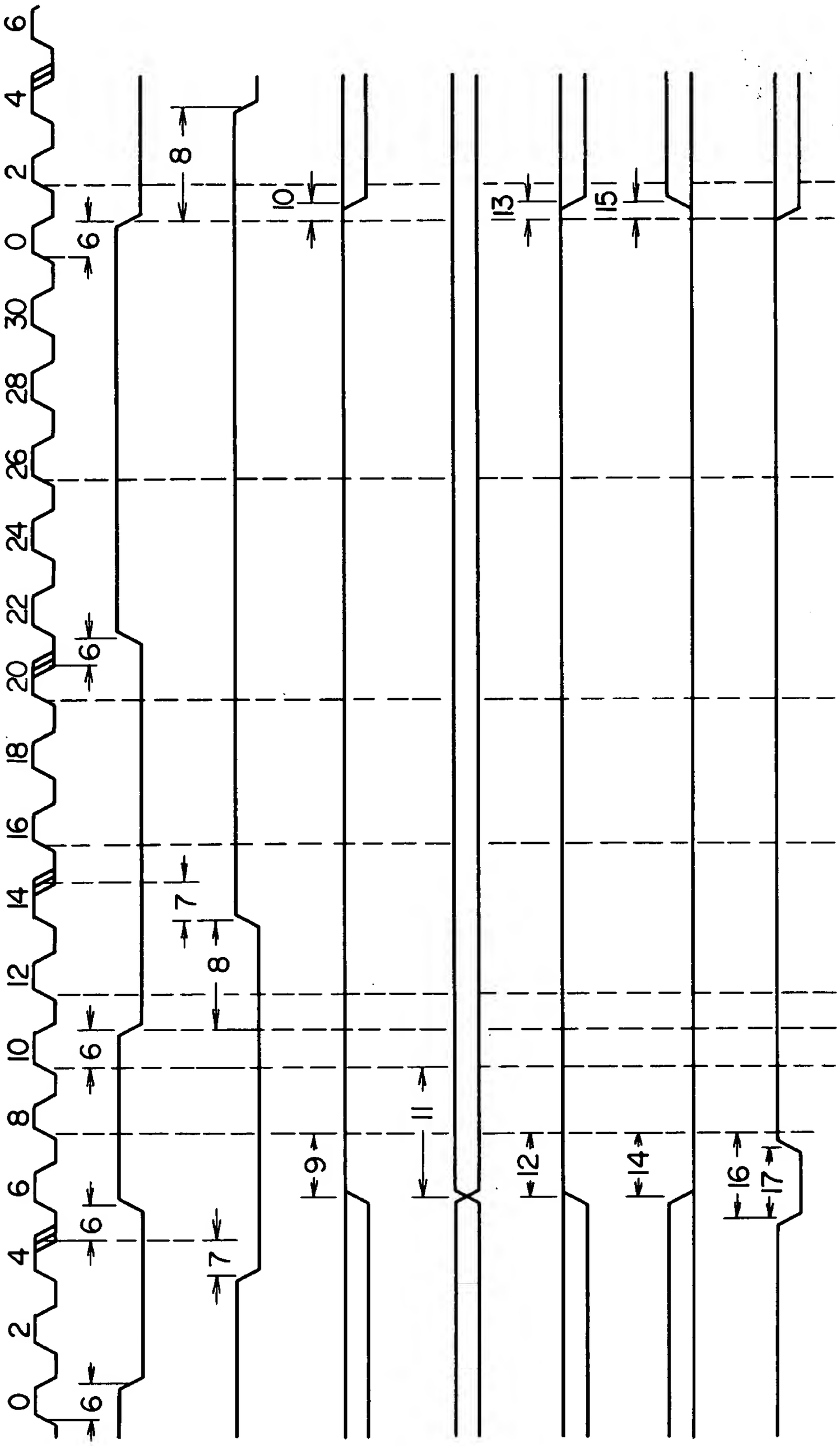


FIG. 16a

FIG. 16b

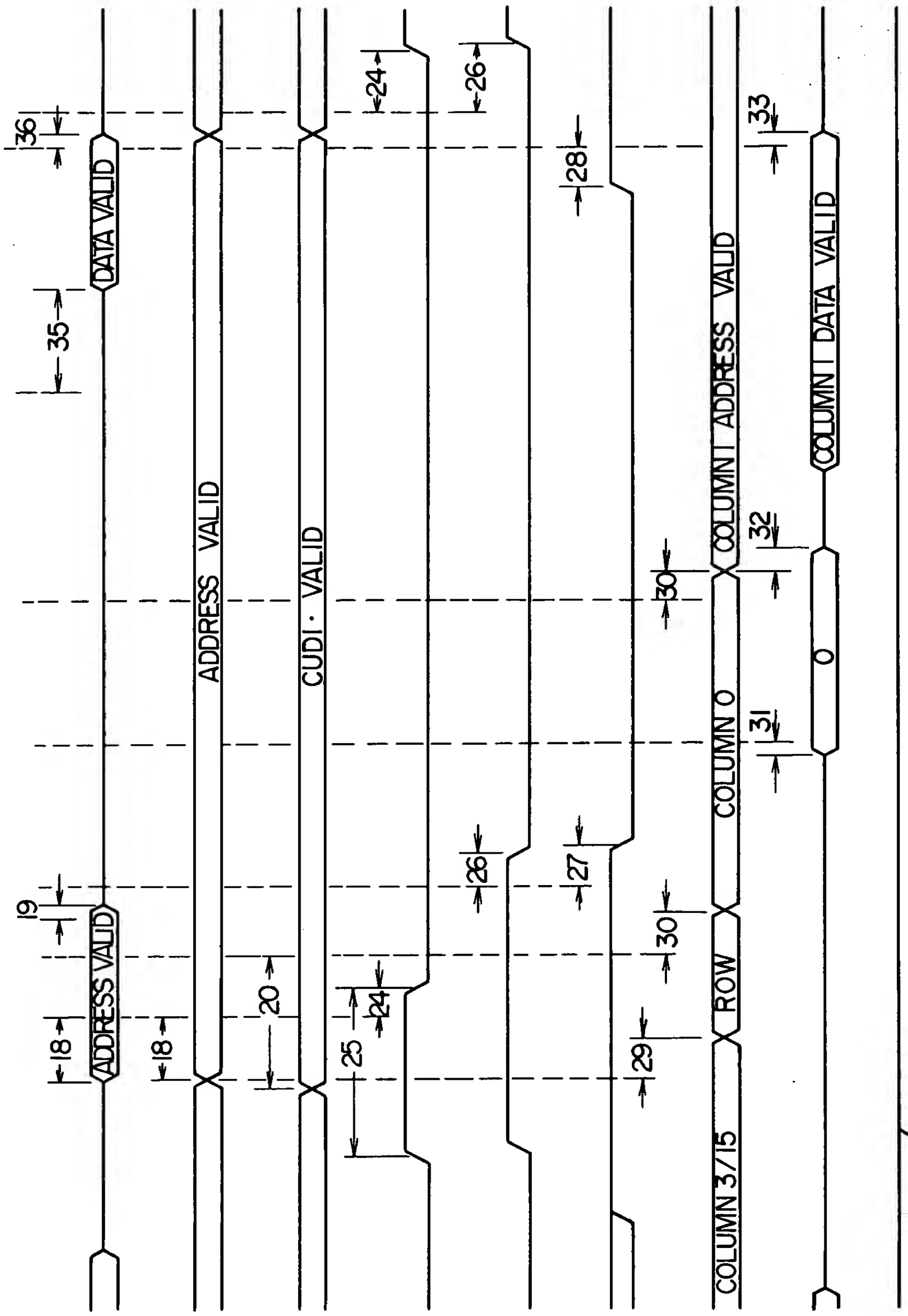

MADO - MAD 15
MA15-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
DATA VALID
CUDI · VALID
COLUMN 3/15
ROW
COLUMN 0
COLUMN 1
0
18
19
20
24
25
26
27
28
29
30
31
32
33
35
36

FIG. 17a

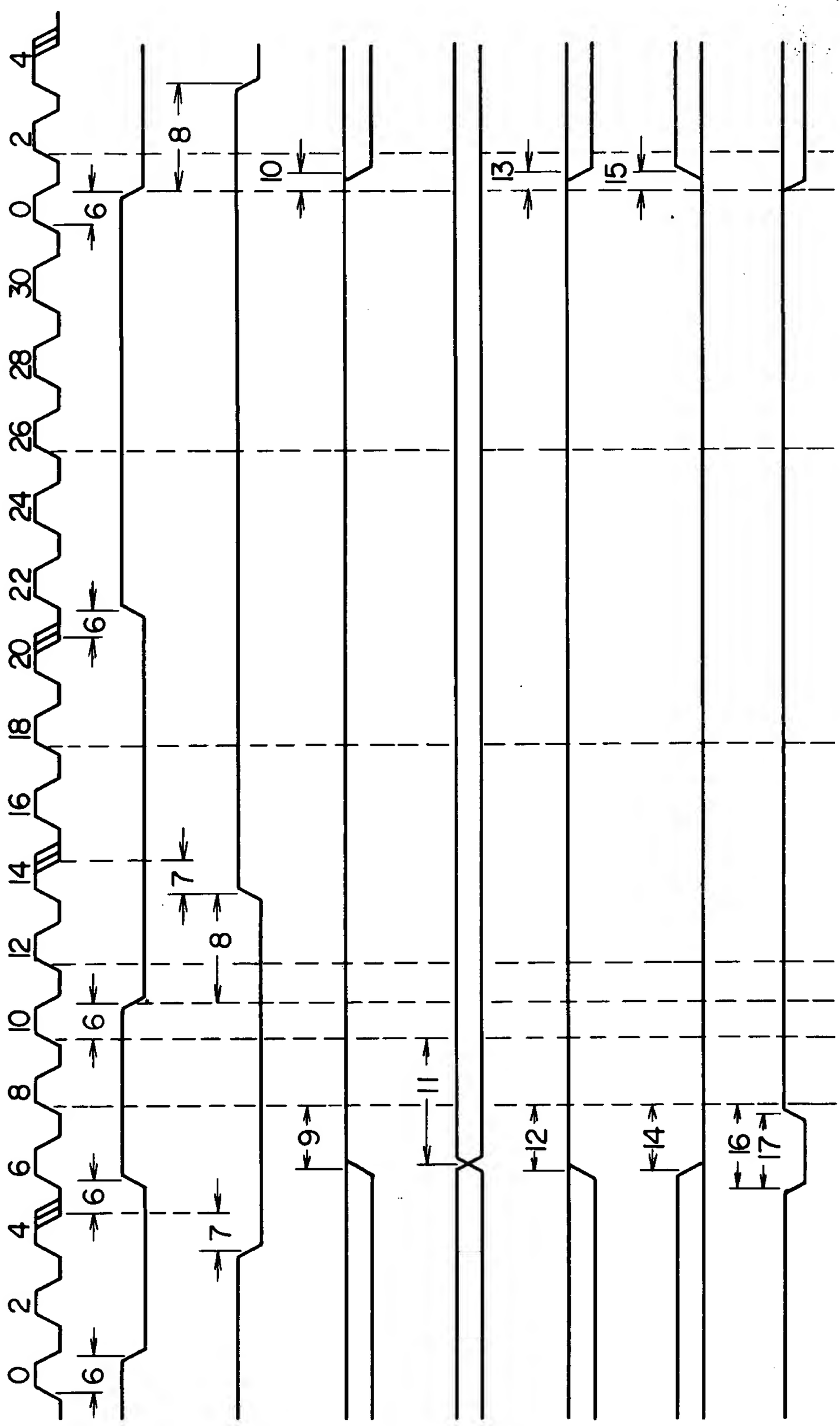

INCLK
2CLK
MCYC
MSYNC
DISPI
MRD
DRAW
AS
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
6
8
10
13
15
7
11
9
12
14
16
17

FIG. 17b

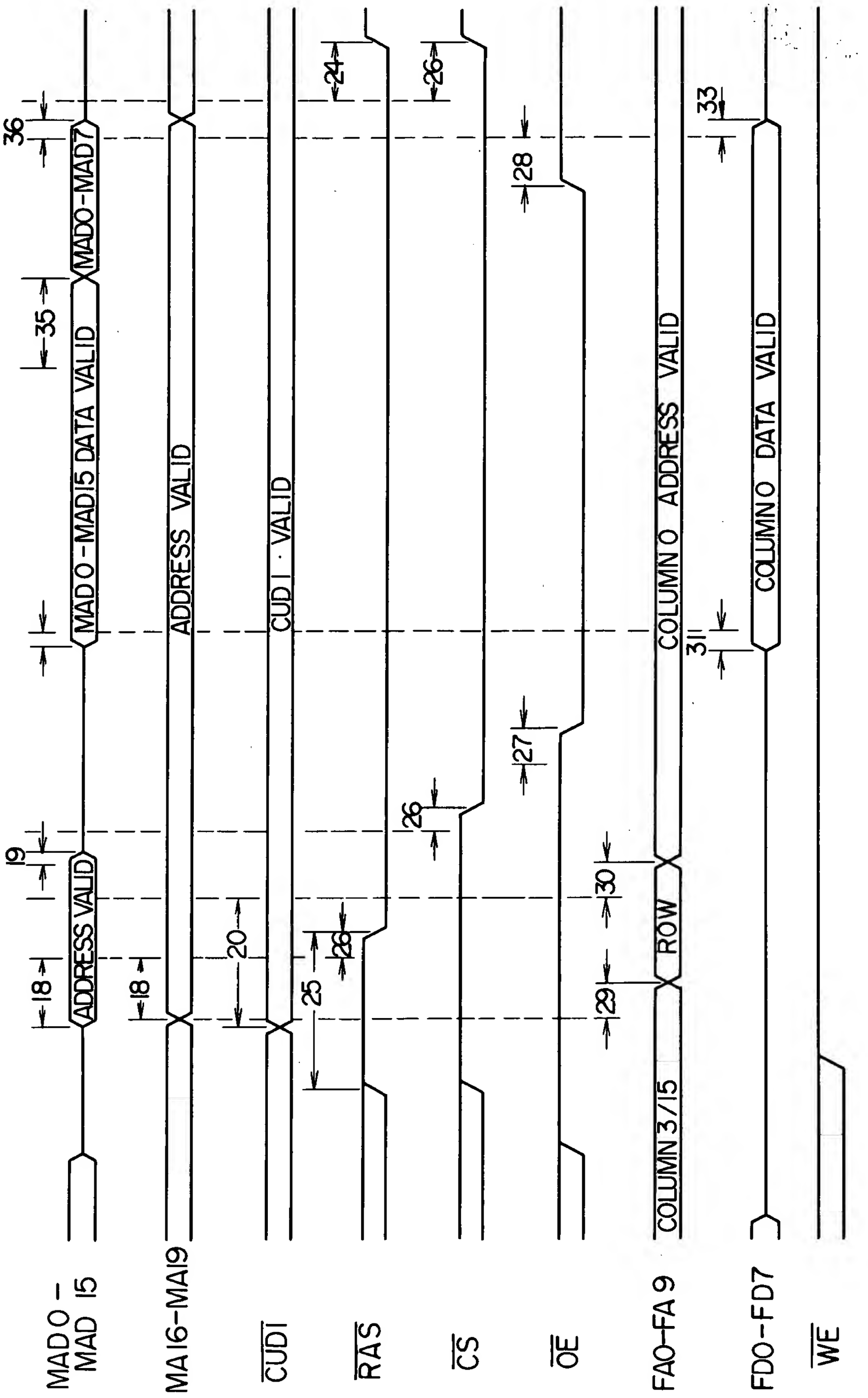

MAD 0 - MAD 15
MA 16-MA19
CUDI
RAS
CS
OE
FA0-FA 9
FD0-FD7
WE
MADO-MAD7
MAD 0-MAD15 DATA VALID
ADDRESS VALID
CUDI · VALID
COLUMN 0 ADDRESS
COLUMN 0 DATA VALID
COLUMN 3/15
ROW
18
19
20
25
26
27
28
29
30
31
33
35
36

FIG. 18a

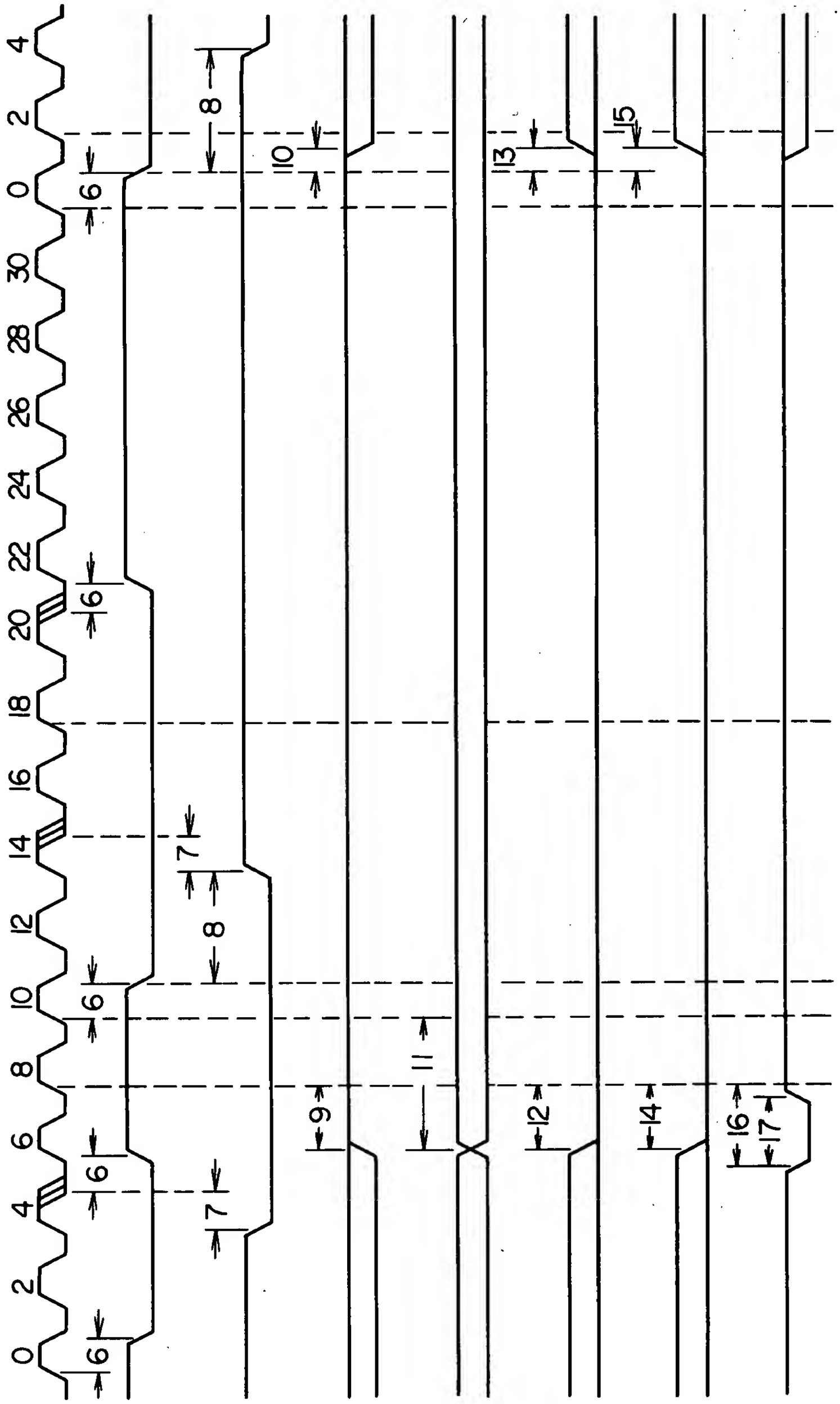

INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
4
2
0
6
8
10
13
15
6
6
7
8
6
11
9
12
14
16
17
6
6
7

FIG. 18b

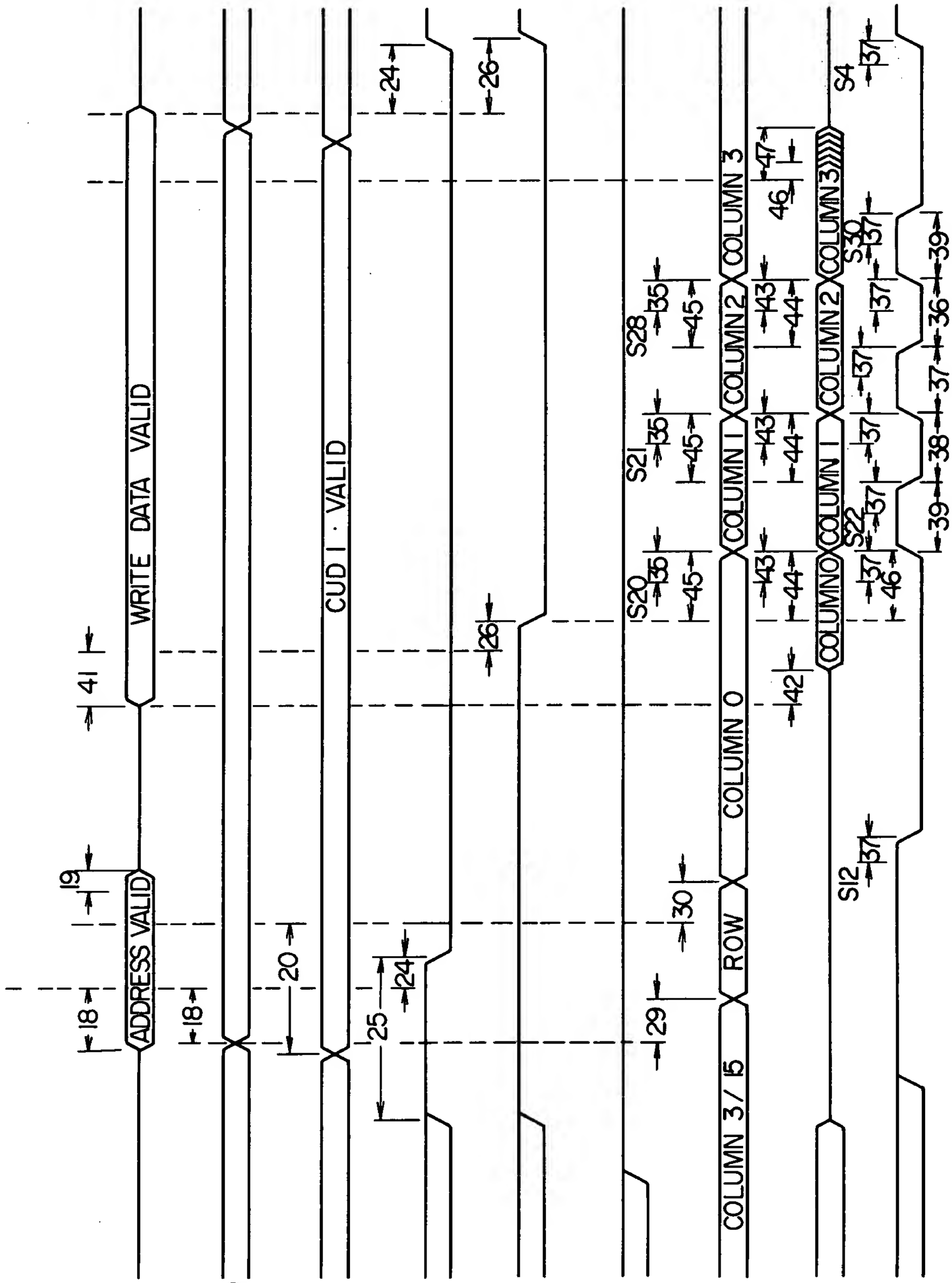

MAD0-MAD15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
WRITE DATA VALID
CUD I · VALID
COLUMN 3/15
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3
ROW
18
19
20
24
25
26
29
30
35
37
38
39
41
42
43
44
45
46
47

FIG. 19a

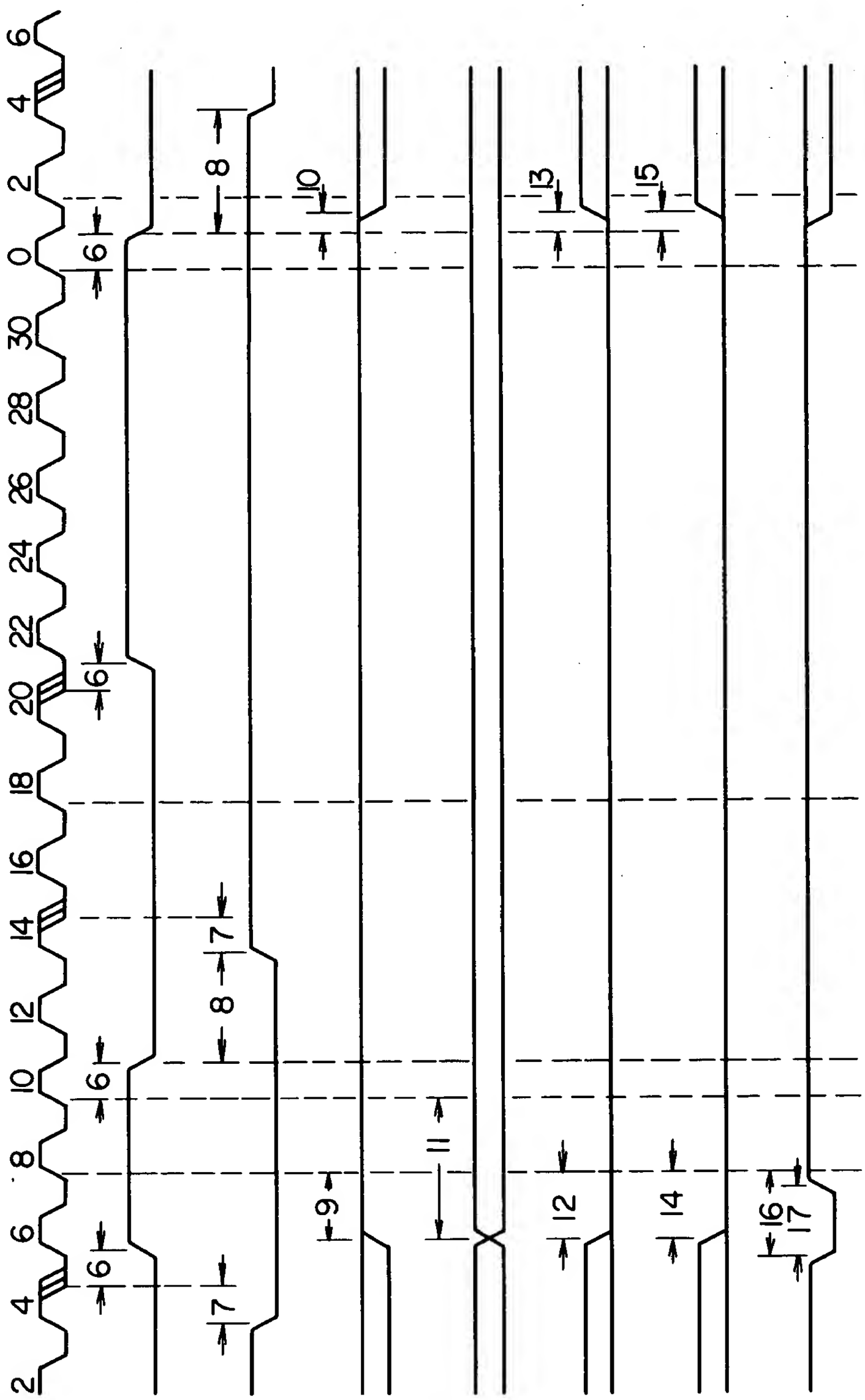


FIG. 19b

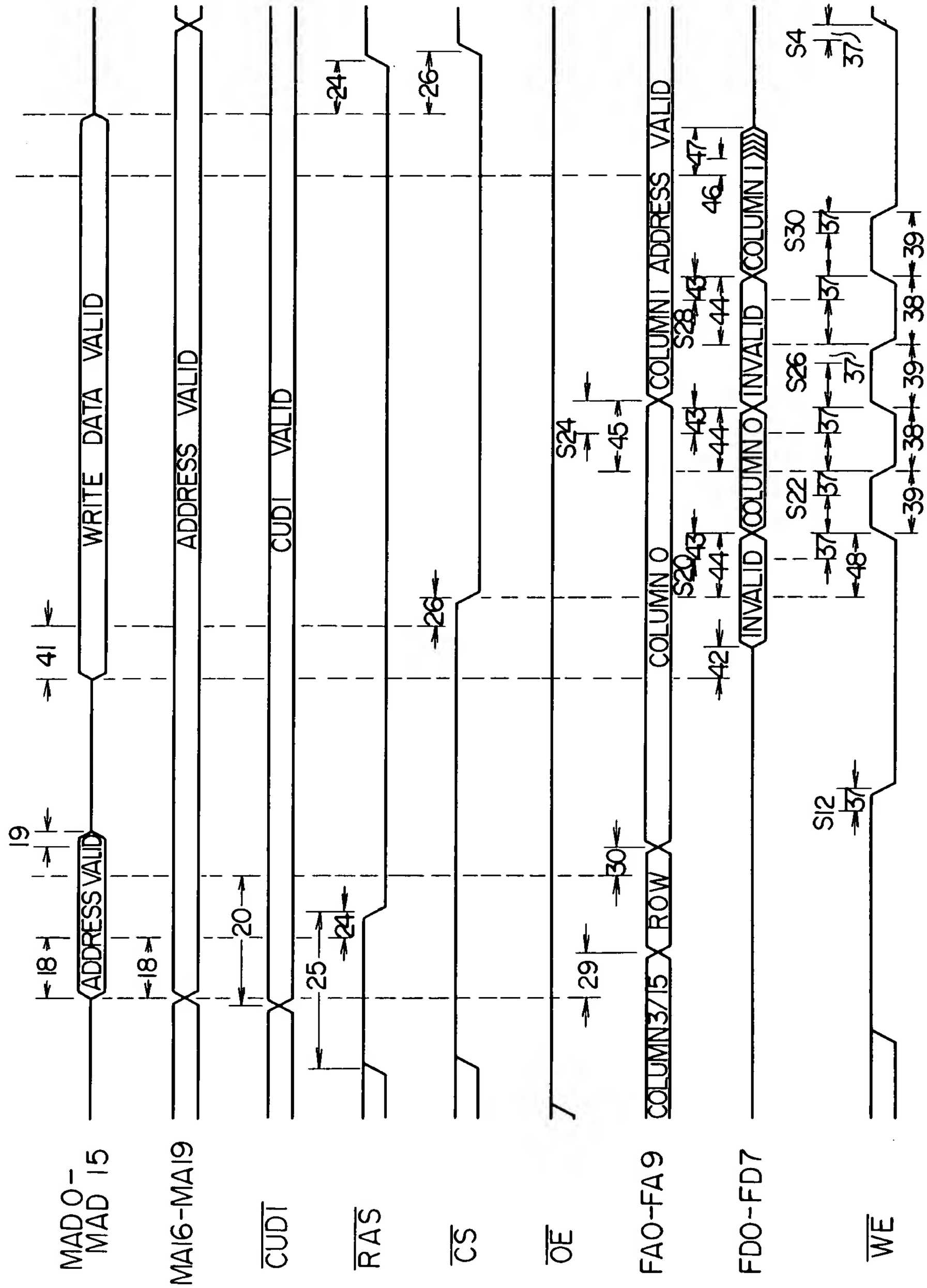

MAD 0-MAD 15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
WRITE DATA VALID
ADDRESS VALID
CUDI VALID
ADDRESS VALID
COLUMN 0
COLUMN I ADDRESS VALID
INVALID COLUMN 0
INVALID COLUMN I
COLUMN 3/15
ROW
18
19
20
24
25
26
29
30
41
42
43
44
45
46
47
48
S4
S30
S28
S26
S24
S22
S20
S12
37
38
39

FIG. 20a

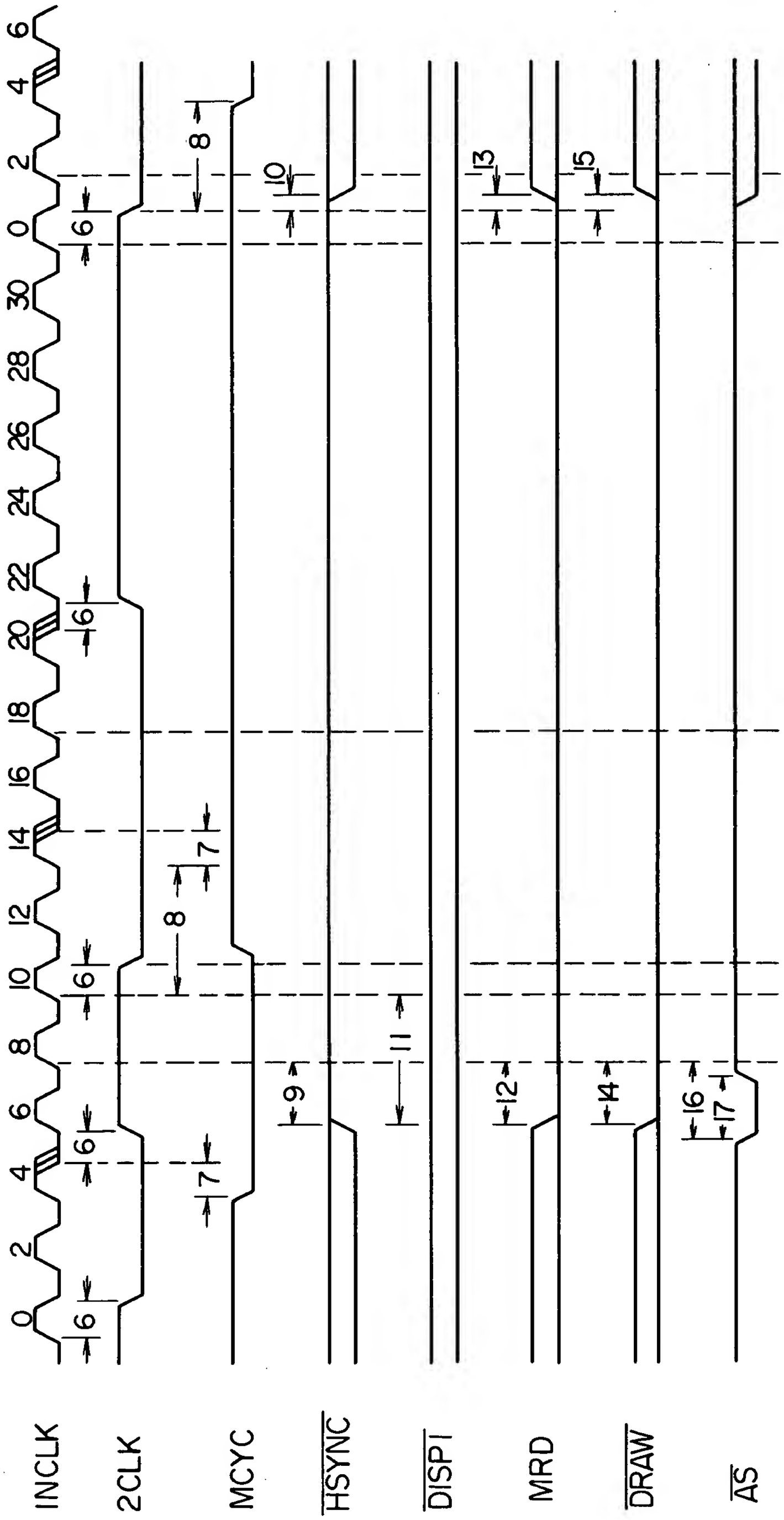

0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
6
8
10
13
15
6
6
6
8
7
6
6
6
7
9
11
12
14
16
17
INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS

FIG. 20b

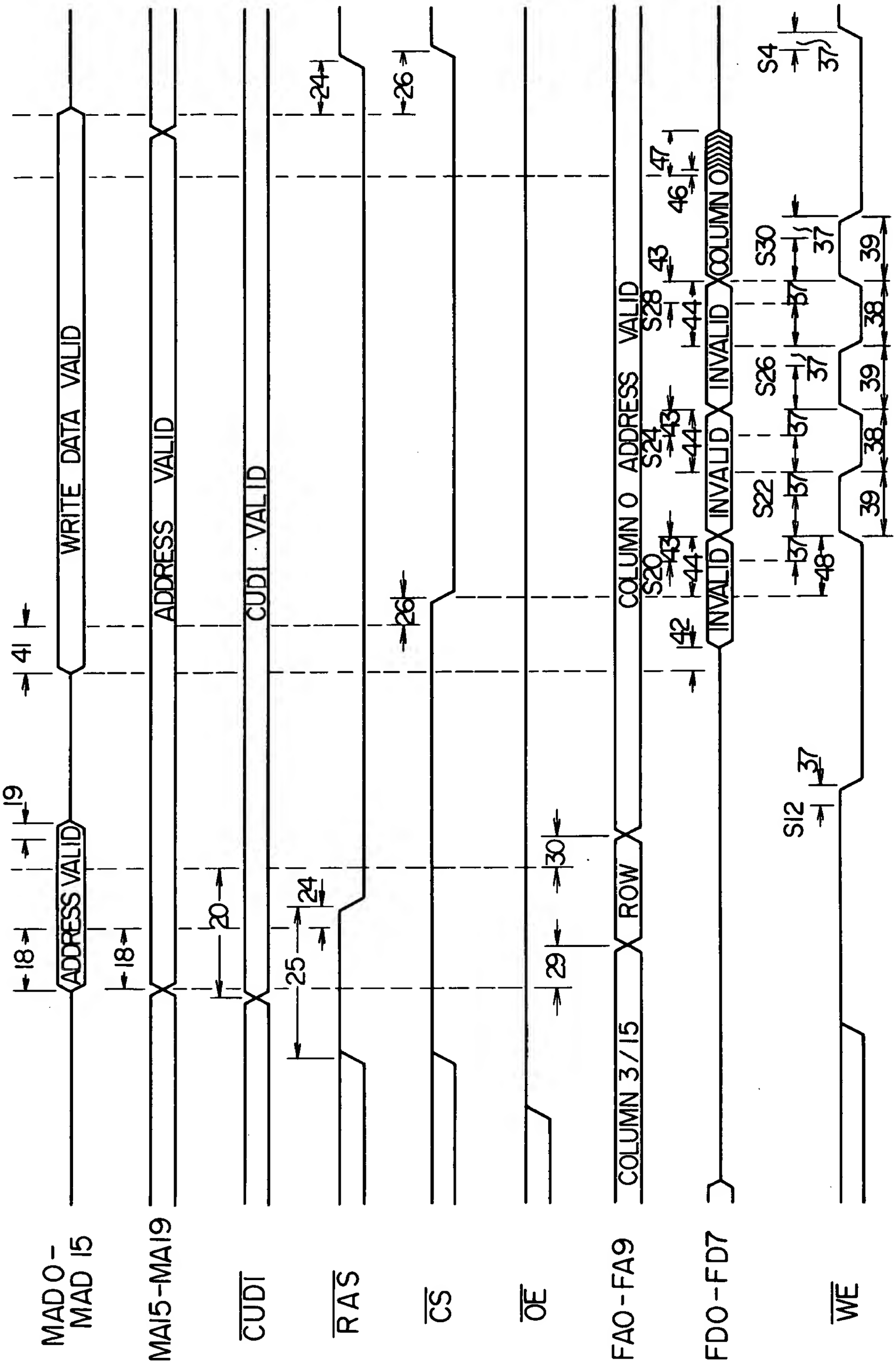

MAD0-MAD15
MA15-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
WRITE DATA VALID
ADDRESS VALID
CUDI VALID
COLUMN ADDRESS VALID
COLUMN 3/15
ROW
INVALID
COLUMN 0
18
19
20
24
25
26
29
30
41
42
43
44
46
47
48
S4
S30
S28
S26
S24
S22
S20
S12
37
38
39

FIG. 21a

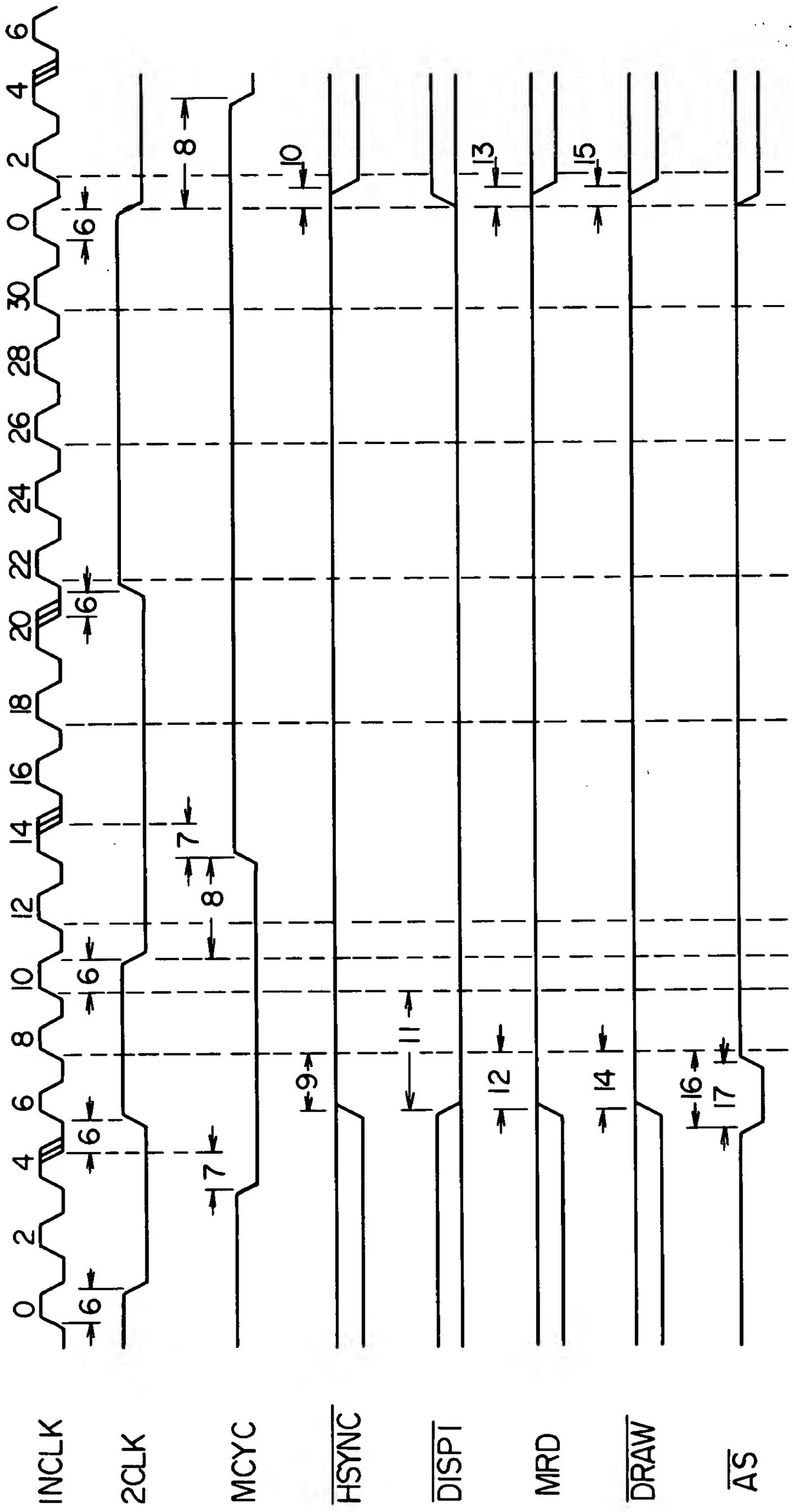

0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
6
8
10
13
15
6
6
7
8
6
6
6
17
9
11
12
14
16
17
INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS

FIG. 21b

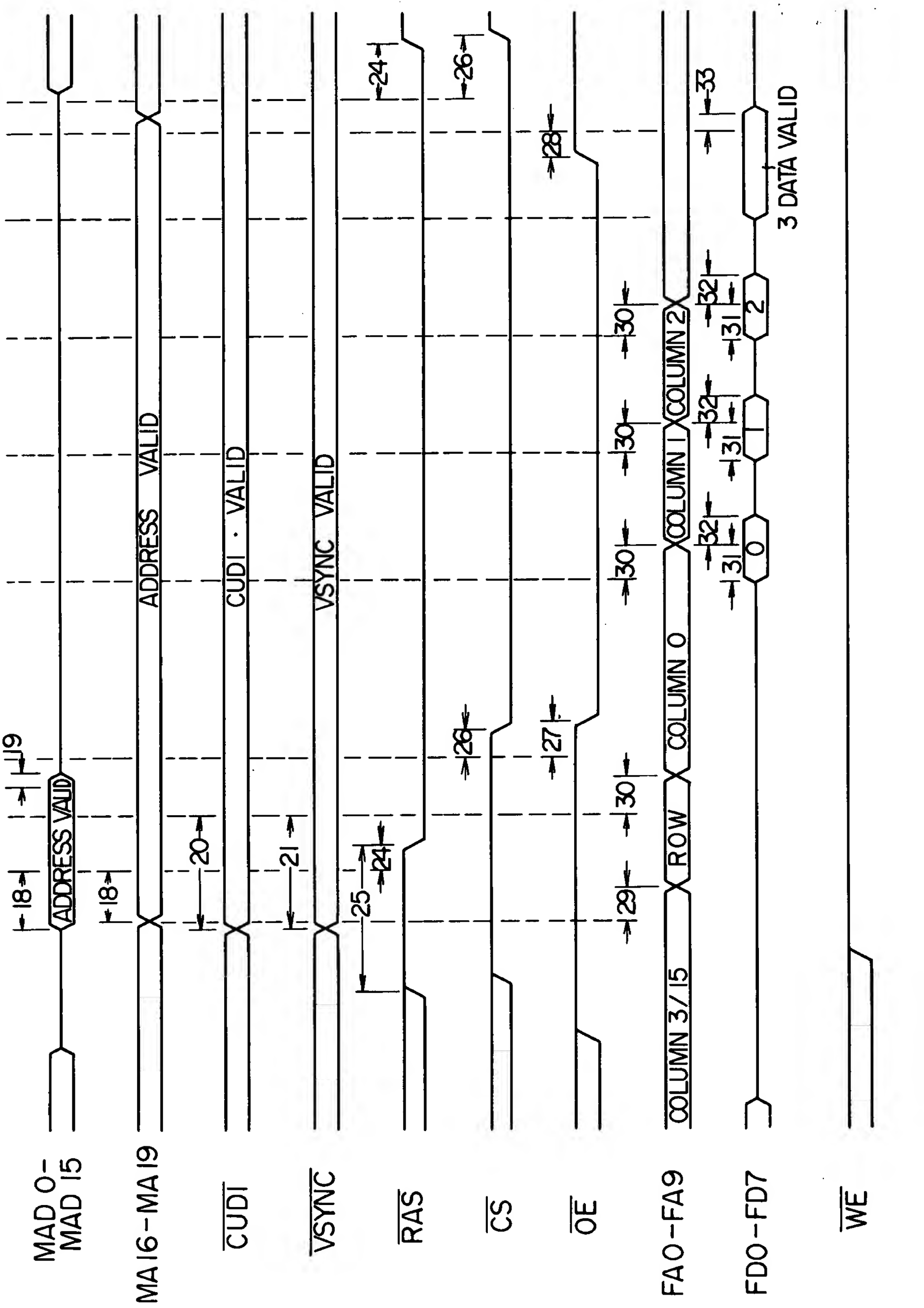

MAD 0-MAD 15
MA 16-MA 19
CUDI
VSYNC
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
ADDRESS VALID
CUDI · VALID
VSYNC VALID
ROW
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3/15
3 DATA VALID
18
19
20
21
24
25
26
27
28
29
30
31
32
33

FIG. 22a

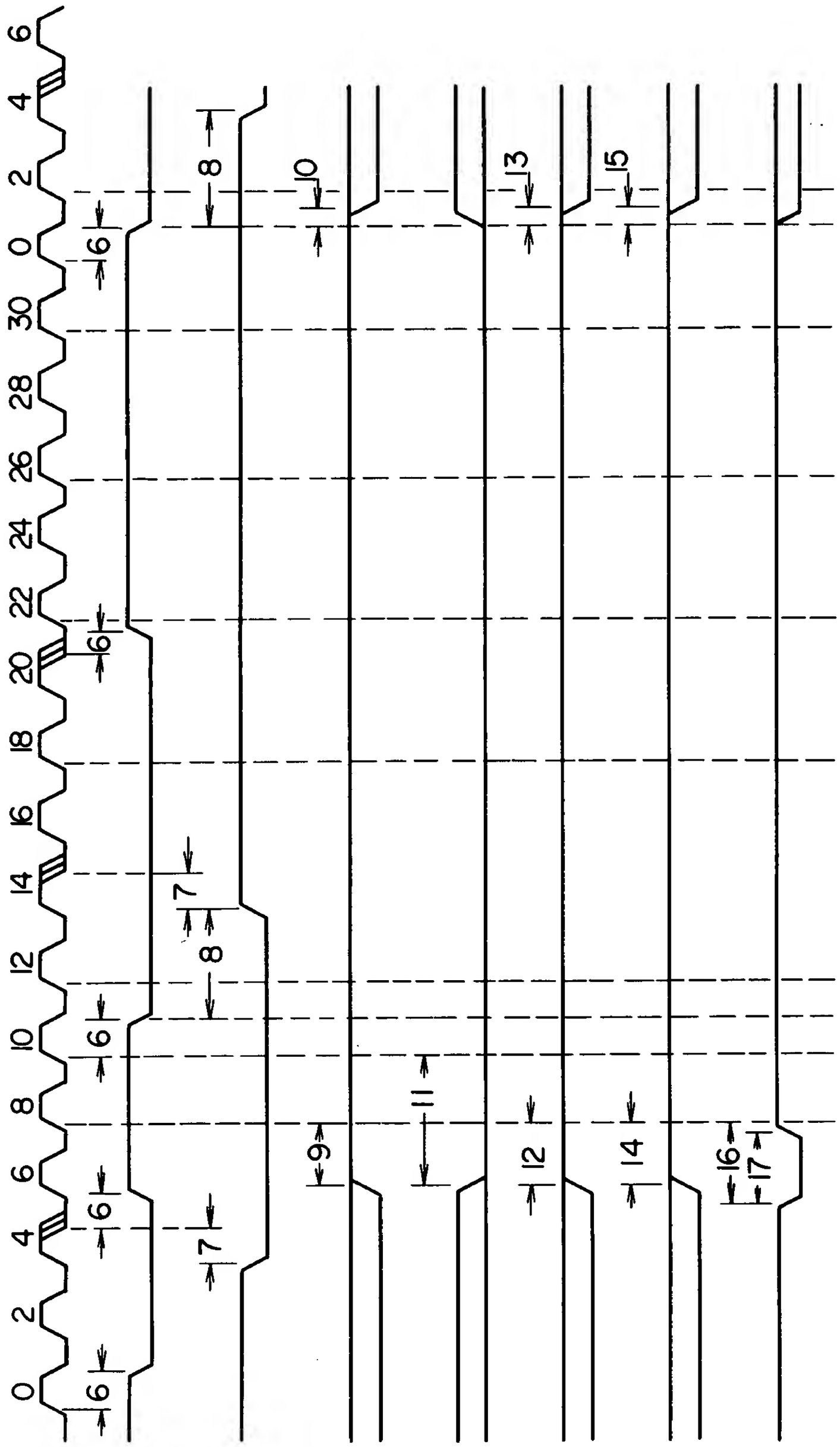

0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
6
8
10
13
15
6
6
7
8
6
6
6
7
9
11
12
14
16
17
INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS

FIG. 22b

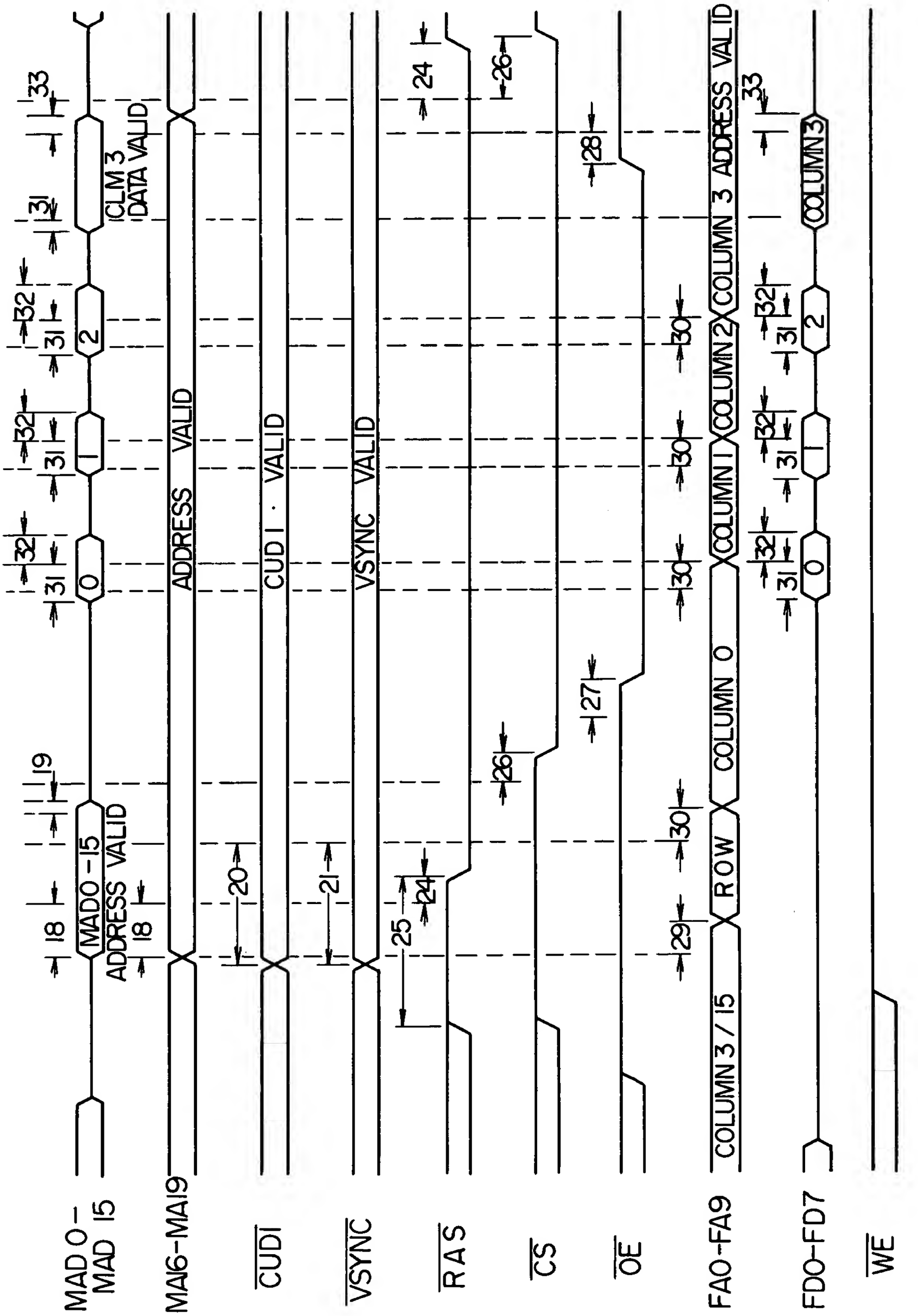

MAD 0–MAD 15
MA16–MA19
CUDI
VSYNC
RAS
CS
OE
FA0–FA9
FD0–FD7
WE
MADO–15
ADDRESS VALID
COLUMN 3 / 15
ROW
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3
CLM 3 DATA VALID
ADDRESS VALID
CUDI · VALID
VSYNC VALID
0
1
2
3
18
19
20
21
24
25
26
27
28
29
30
31
32
33

FIG. 23a

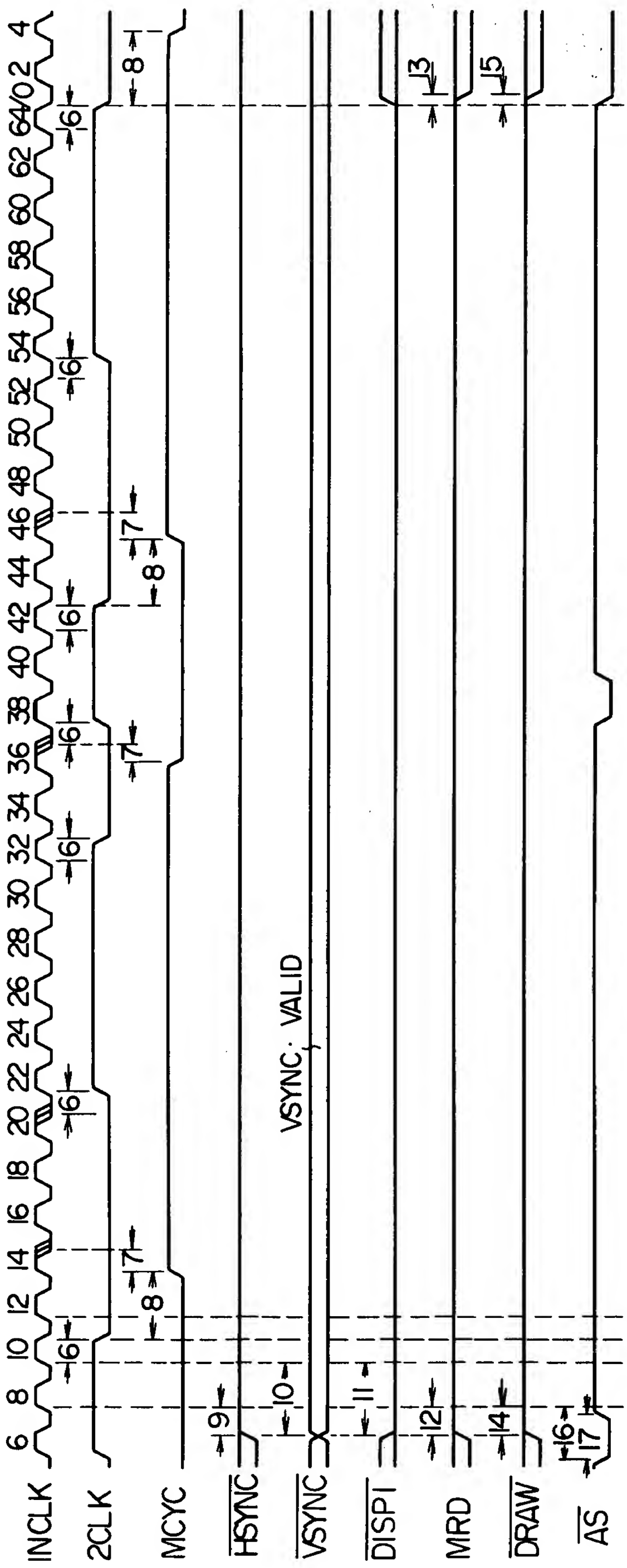

4
2
0
64
62
60
58
56
54
52
50
48
46
44
42
40
38
36
34
32
30
28
26
24
22
20
18
16
14
12
10
8
6
8
3
5
6
7
8
9
10
11
12
14
16
17
INCLK
2CLK
MCYC
HSYNC
VSYNC
DISPI
MRD
DRAW
AS
VSYNC: VALID

FIG. 23b

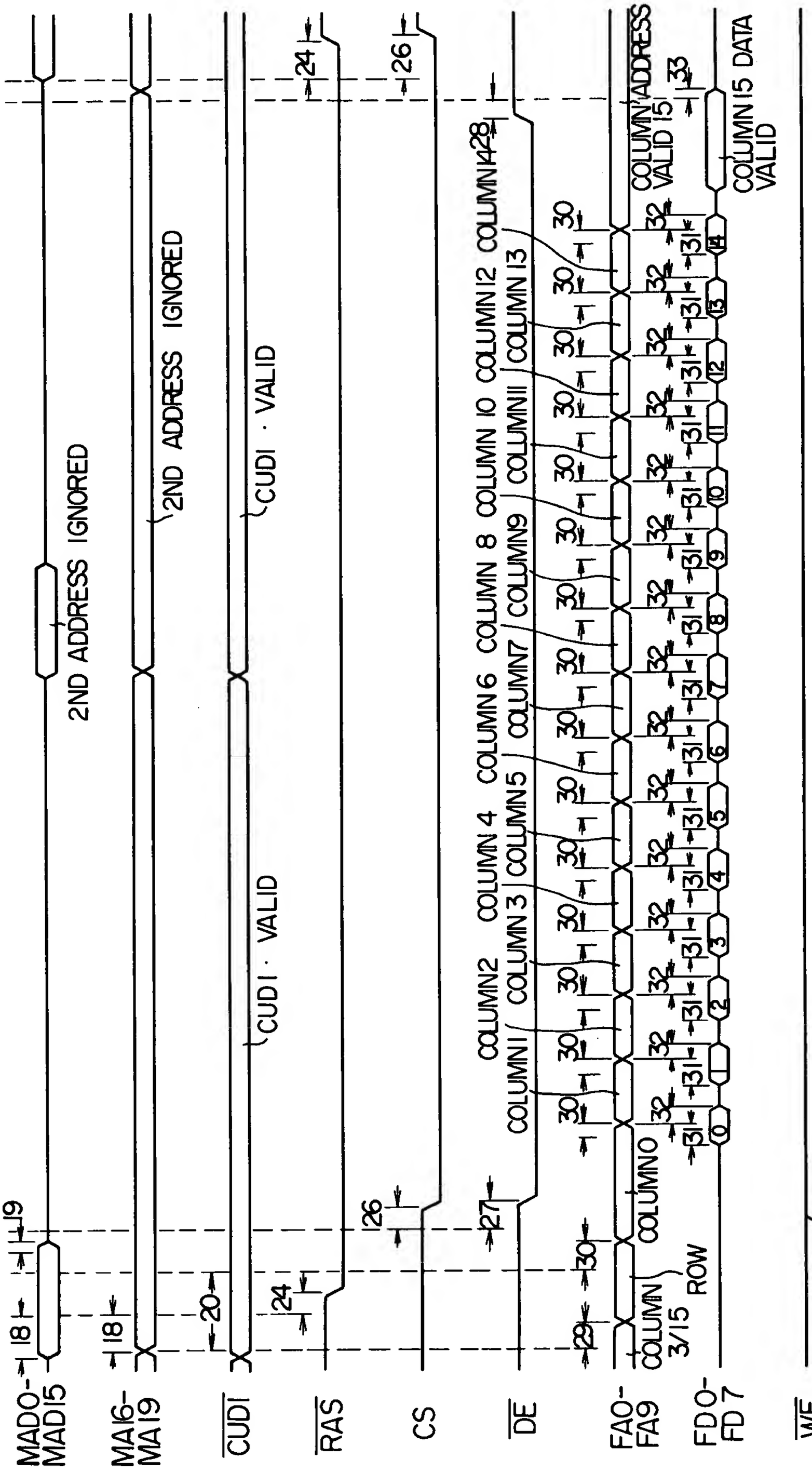

MAD0-MAD15
MA16-MA19
CUDI
RAS
CS
DE
FA0-FA9
FD0-FD7
WE
2ND ADDRESS IGNORED
CUDI · VALID
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3
COLUMN 4
COLUMN 5
COLUMN 6
COLUMN 7
COLUMN 8
COLUMN 9
COLUMN 10
COLUMN 11
COLUMN 12
COLUMN 13
COLUMN 14
COLUMN 15
COLUMN ADDRESS VALID
COLUMN 15 DATA VALID
ROW
COLUMN 3/15

FIG. 24a

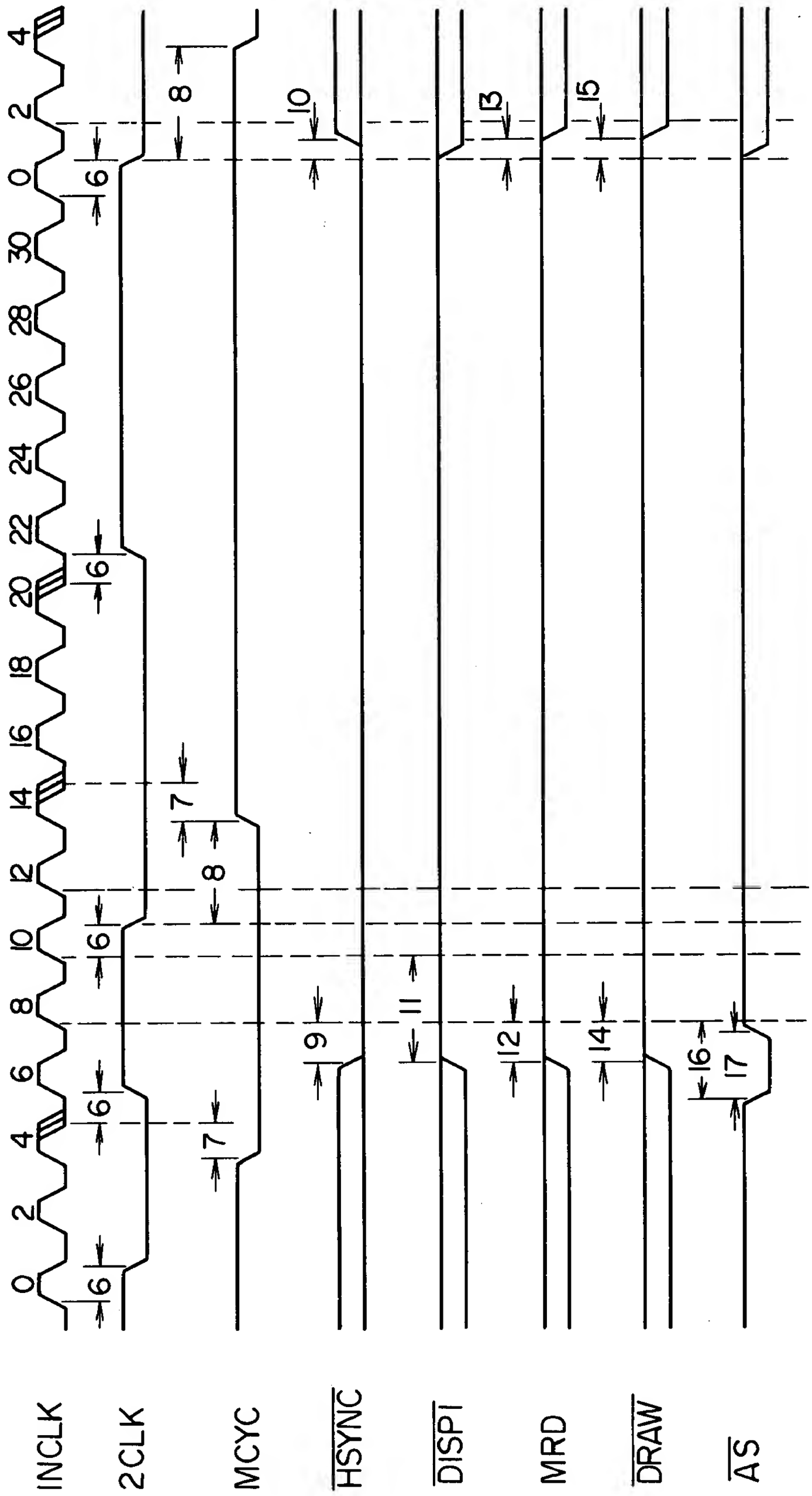

INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
4
2
0
6
8
10
13
15
6
6
6
6
6
7
8
6
7
9
11
12
14
16
17

FIG. 24b

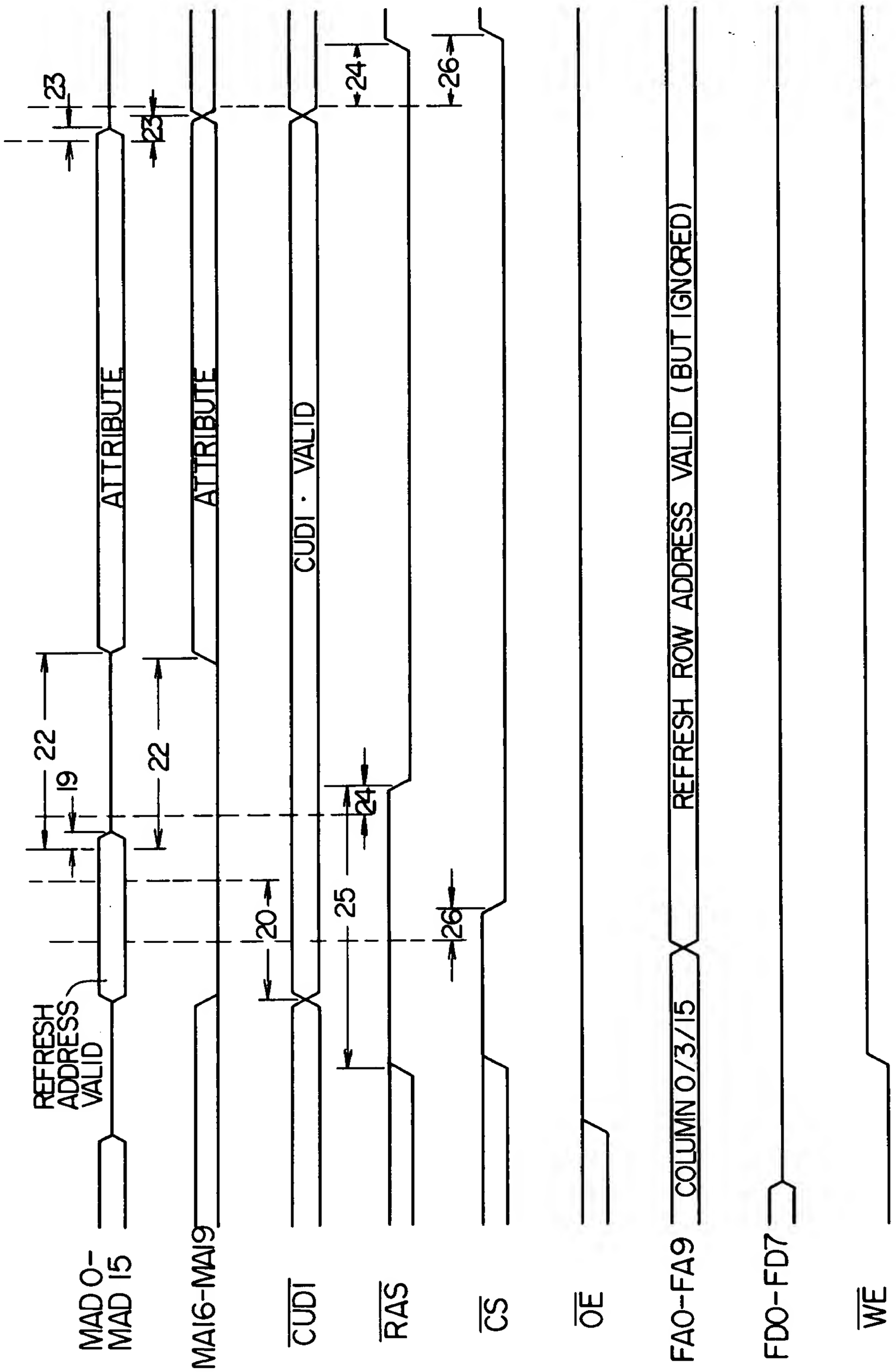

MAD 0-
MAD 15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
REFRESH
ADDRESS
VALID
ATTRIBUTE
ATTRIBUTE
CUDI · VALID
REFRESH ROW ADDRESS VALID (BUT IGNORED)
COLUMN 0/3/15
23
23
24
26
22
19
22
24
20
25
26

FIG. 25

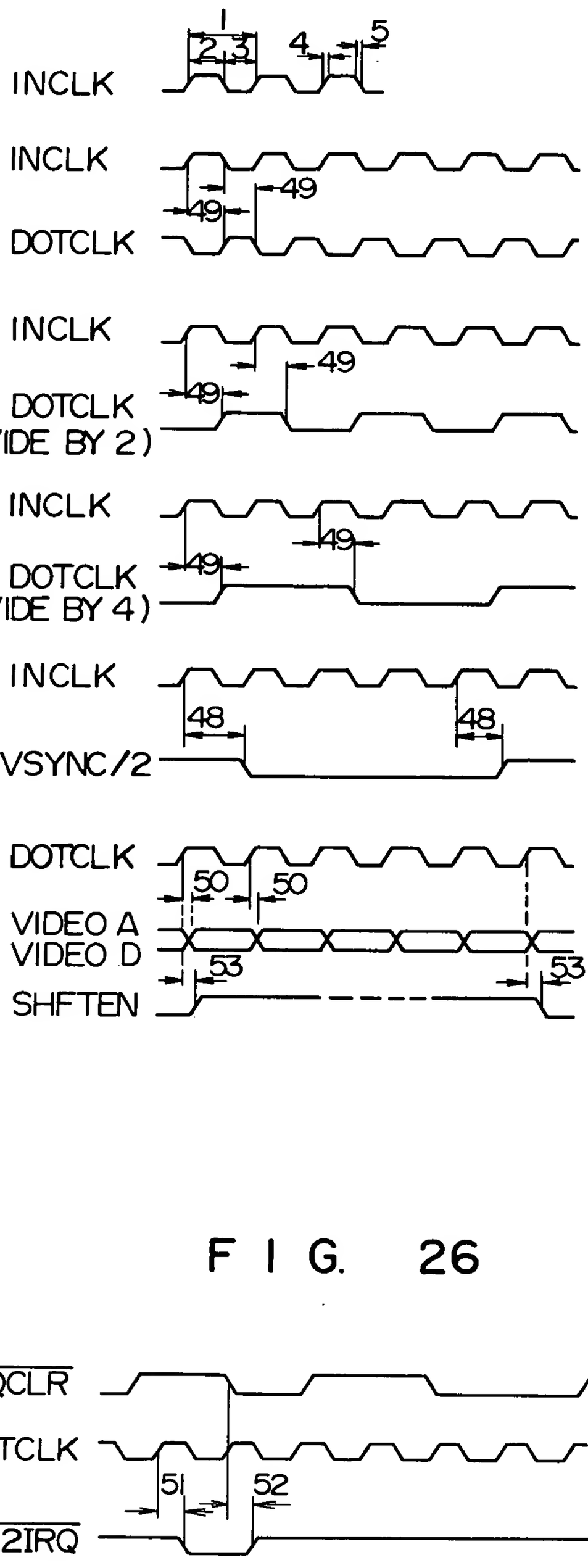

INCLK
1
2
3
4
5
INCLK
49
49
DOTCLK
INCLK
49
49
DOTCLK
(DIVIDE BY 2)
INCLK
49
49
DOTCLK
(DIVIDE BY 4)
INCLK
48
48
VSYNC/2
DOTCLK
50
50
VIDEO A
VIDEO D
53
53
SHFTEN

FIG. 26

IRQCLR
DOTCLK
51
52
BL2IRQ

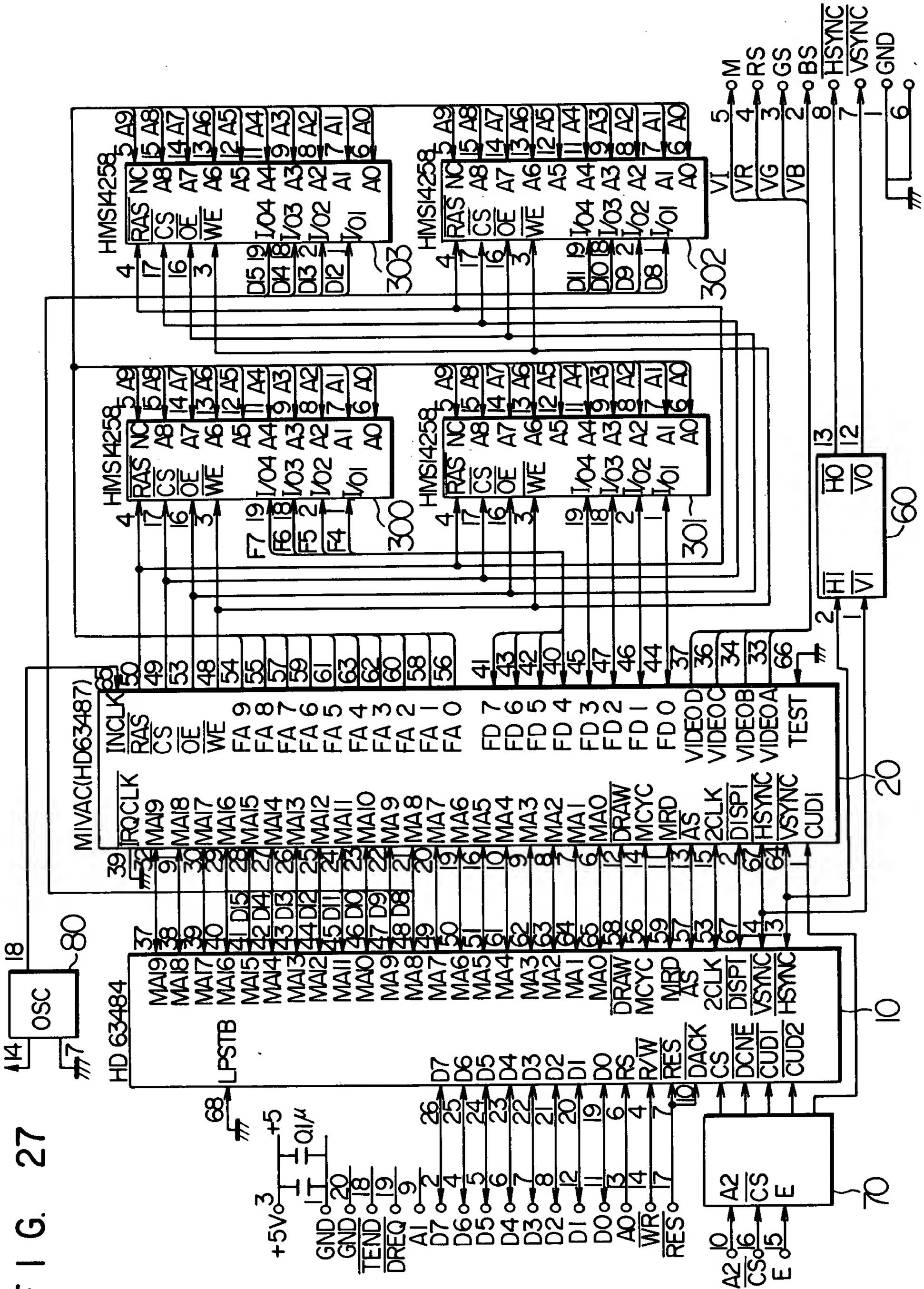

HMS14258
HD 63484
MIVAC(HD63487)
OSC
M
RS
GS
BS
HSYNC
VSYNC
GND
VI
VR
VG
VB
HO
VO
HI
VI
60
20
10
80
70
300
301
302
303

FIG. 27

FIG. 28

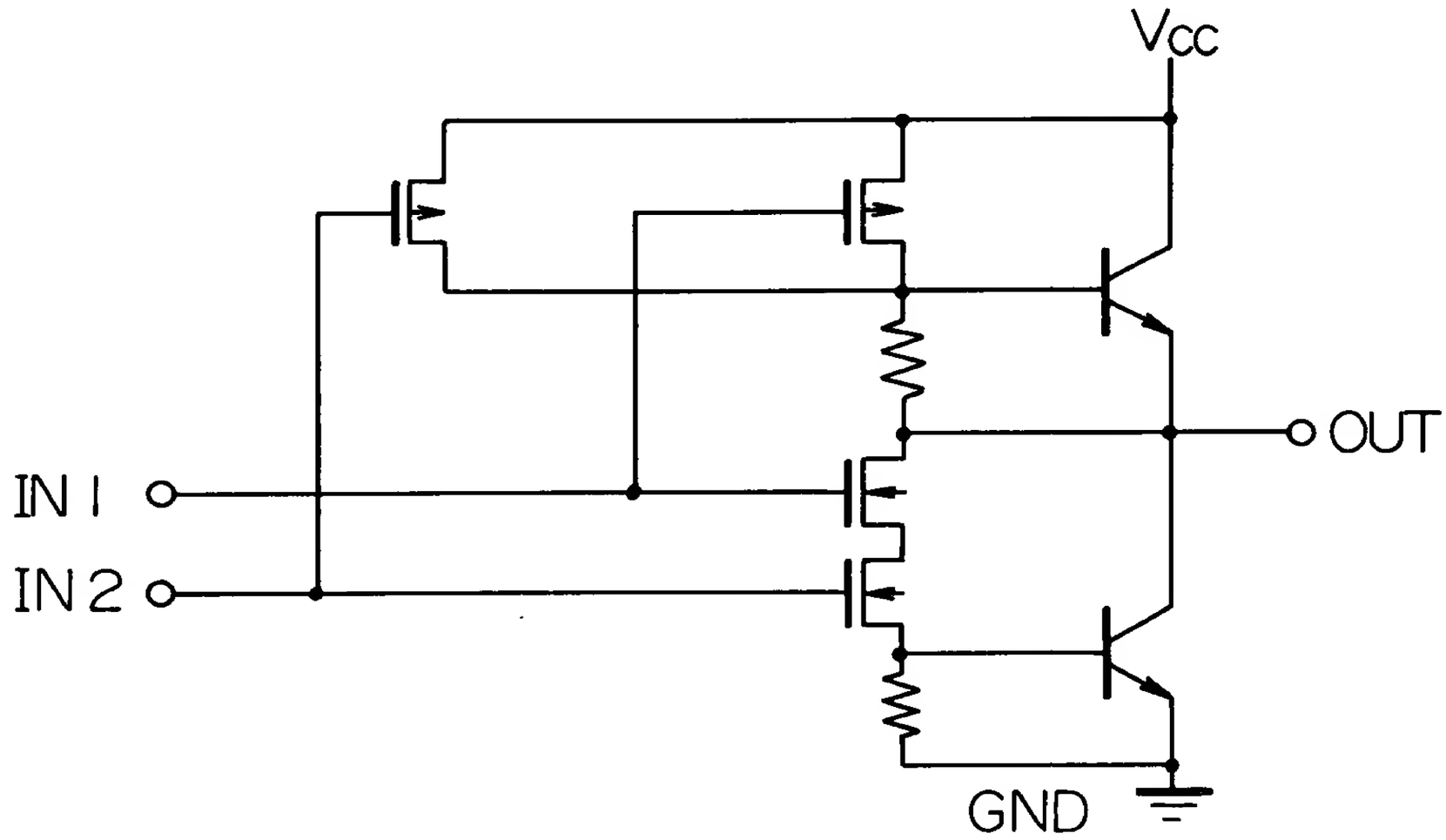


FIG. 29a

FA	4 ACCESSES / MCYC (DRAW, DISPLAY)				16 ACCESSES / 2 MCYCS (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	—	—	MAD 8	NC0	—	—	MAD 8	NC0
8	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1
7	MAD 8	NC2	MA 17	MAD 7	MAD 8	NC2	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC0

[ ] : COLUMN ADDRESS COUNTER

FIG. 29b

FA	2 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)				16 ACCESSES / 2MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	NCO	-	-	MA 18	NCO	-	-	MA 18	NCO
8	MAD 9	NC1	MAD 9	MAD 8	MAD 9	NC1	MAD 9	MAD 8	MAD 9	NC1	MAD 9	MAD 8
7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 14
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	WC 2	MAD 12	WC 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC 1	MAD 11	WC 1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC 0	MAD 10	WC 0	MAD 10	WC 0	MAD 10	WC 0

[ ] : COLUMN ADDRESS COUNTER

FIG. 29c

FA	1 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	—	—	MA 18	MAD 9	—	—	MA 18	MAD 9
8	MAD 9	MAD 8	MA 19	MAD 8	MAD 9	MAD 8	MA 19	MAD 8
7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7	MAD17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC 1	MAD 11	WC 1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC 0	MAD 10	WC 0

[ ]: COLUMN ADDRESS COUNTER